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MT6757 LTE-A Smartphone Application Processor Technical Brief

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Preface

Acronyms for register types

R/W For both read and write access

RO Read only

RC Read only. After the register bank is read, every bit that is HIGH(1) will be cleared to LOW(0) automatically.

WO Write only

W1S Write only. When data bits are written to the register bank, every bit that is HIGH(1) will cause the corresponding bit to be set to 1. Data bits that are LOW(0) have no effects on the corresponding bit.

W1C Write only. When data bits are written to the register bank, every bit that is HIGH(1) will cause the corresponding bit to be cleared to 0. Data bits that are LOW(0) have no effects on the corresponding bit.

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1 System Overview

The MT6757 device (see Figure 1-1), with integrated Bluetooth, FM, WLAN and GPS modules, is a highly integrated baseband platform incorporating both modem and application processing subsystems to enable LTE/LTE-A and C2K smart phone applications. The chip integrates ARM® Cortex-A53 operating up to 2.35GHz, an ARM® Cortex-R4 MCU and powerful multi-standard video codec. In addition, an extensive set of interfaces and connectivity peripherals are included to interface to cameras, touch-screen displays and MMC/SD cards.

The application processor, an Octa-core ARM® Cortex-A53 MPCore™ equipped with NEON engine offers processing power necessary to support the latest OpenOS along with its demanding applications such as web browsing, email, GPS navigation and games. All are viewed on a high resolution touch screen display with graphics enhanced by the 2D and 3D graphics acceleration.

The multi-standard video accelerator and an advanced audio subsystem are also integrated to provide advanced multimedia applications and services such as streaming audio and video, a multitude of decoders and encoders.

ARM® Cortex-R4, DSP, and 2G and 3G coprocessors combined provide a powerful modem subsystem capable of supporting LTE Cat 6, Category 24 HSDPA downlink and Category 7 HSUPA uplink data rates, Category 14 TD-HSDPA downlink and Category 6 TD-HSUPA uplink, as well as Class 12 GPRS, EDGE.

MT6757 also embodies wireless communication device, including WLAN, Bluetooth and GPS. With four advanced radio technologies integrated into one single chip, MT6757 provides the best and most convenient connectivity solution in the industry.

The enhanced overall quality is achieved for simultaneous voice, data and audio/video transmission on mobile phones and Media Tablets. The small footprint with low-power consumption greatly reduces the PCB layout resource.

1.1 Highlighted Features Integrated in MT6757

- Quad-core ARM® Cortex-A53 MPCore™ operating at 2.35GHz and the other quad-core ARM® Cortex-A53 MPCore™ operating at 1.64GHz
- LPDDR3 up to 4GB (LPDDR3-1866)
- LPDDR4 up to 6GB (LPDDR4-3200)
- LTE Cat 6 (300Mps)
- Embedded connectivity system including WLAN/BT/FM/GPS
- Resolution up to FHD (1,920*1,080)
- OpenGL ES 3.0 3D graphic accelerator
- ISP supports 21MP@30fps.
- HEVC 4K @ 30fps decoder
- H.264 4K @ 30fps encoder
- Speech codec (FR, HR, EFR, AMR FR, AMR HR and Wide-Band AMR)

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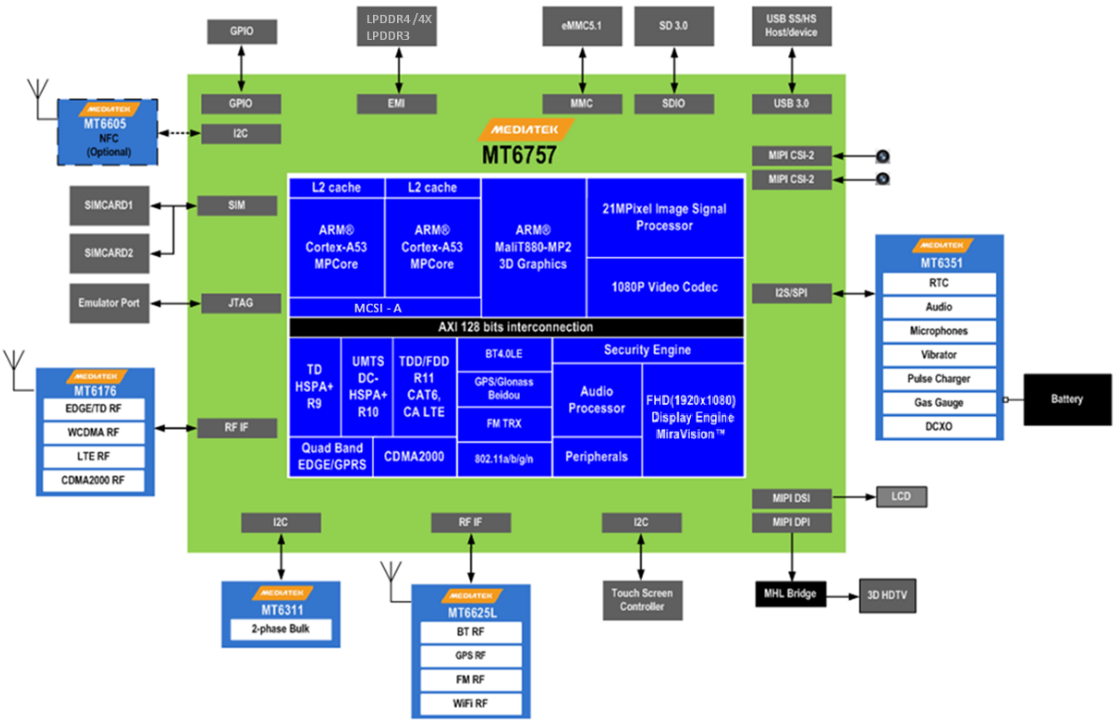

Figure 1-1. High-level MT6757 functional block diagram

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1.2 Platform Features

- **General**
  - Smartphone, two MCU subsystems architecture
  - eMMC boot support
  - Supports LPDDR3
  - Supports LPDDR4/LPDDR4X

- **AP MCU subsystem**
  - Quad-core ARM® 2.35GHz Cortex-A53 MPCoreTM and another quad-core ARM® 1.64GHz Cortex-A53 MPCoreTM
  - NEON multimedia processing engine with SIMDv2/VFPv4 ISA support
  - 32KB L1 I-cache and 32KB L1 D-cache for each cluster
  - 512KB L2 cache for each cluster
  - DVFS technology with adaptive operating voltage from 0.6V to 1.025V

- **MD MCU subsystem**
  - Two ARM® Cortex-R4 processors with max. 800 MHz operation frequency
  - 64KB I-cache, 64KB D-cache
  - 512KB TCM (tightly-coupled memory)
  - Coresonic DSP for running LTE modem tasks
  - FD216 DSP for running modem/voice tasks, with max. 312MHz operation frequency
  - High-performance AXI and AHB bus
  - General DMA engine and dedicated DMA channels for peripheral data transfer
  - Watchdog timer for system error recovery
  - Power management for clock gating control

- **MD external interfaces**
  - Dual SIM/USIM interface
  - Interface pins with RF and radio-related peripherals (antenna tuner, PA, etc.)

- **Security**
  - ARM® TrustZone® Security

- **External memory interface**
  - LPDDR3 up to 4GB (LPDDR3-1866)
    Single channel with 32-bit data bus width
  - LPDDR4/LPDDR 4X up to 6GB (LPDDR4-3200/LPDDR4X-3200)
    Dual channel with 32-bit data bus width
  - Self-refresh/partial self-refresh mode
  - Low-power operation
  - Programmable slew rate for memory controller's IO pads
  - Dual rank memory device
  - Advanced bandwidth arbitration control

- **Peripherals**
  - USB3.0 SS device support
  - USB2.0 OTG mode
  - eMMC5.1
  - 2 UART for debugging and applications
  - 6 SPI masters for external devices
  - 5 I2C to control peripheral devices, e.g. CMOS image sensor, LCM or FM receiver module
  - Max. 3 PWM channels (depending on system configuration/IO usage)
  - I2S for connection with optional external hi-end audio codec
  - GPIOs
  - 3 sets of memory card controllers supporting SD/SDHC/MS/MSPRO/MMC and SDIO2.0/3.0 protocols

- **Operating conditions**
  - Core voltage: 0.7V/0.8V
  - I/O voltage: 1.8V/2.8V/3.3V
  - Memory: 1.1V/0.6V (LPDDR4X optional)
  - LCM interface: 1.8V
  - Clock source: 26MHz, 32.768kHz

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- **Package**
  - Type: VFBGA
  - 13.0mm*13.4mm
  - Height: Max. 0.9mm
  - Ball count: 771 balls
  - Ball pitch: 0.4mm

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1.3 Modem Features

- **LTE**
  - FDD/TDD Up to 300Mbps downlink, 50Mbps uplink
  - Downlink carrier aggregation (CA) ability; 1.4 to 20MHz RF bandwidth per component carrier (CC) and up to 2 CCs
  - 8*2 downlink SU-MIMO per component carrier
  - Downlink MU-MIMO per component carrier
  - Supports feICIC
  - Supports MBMS
  - Uplink CoMP ability

- **3G UMTS FDD supported features**
  - 3G modem supports most main features in 3GPP Release 7 and Release 8
  - CPC (DTX in CELL_DCH, UL DRX DL DRX), HS-SCCH-less, HS-DSCH
  - Dual cell operation
  - MAC-ehs
  - 2 DRX (receiver diversity) schemes in URA_PCH and CELL_PCH
  - Uplink Cat. 7 (16QAM), throughput up to 11.5Mbps
  - Downlink Cat. 24 (64QAM, dual-cell HSDPA), throughput up to 42.2Mbps
  - Fast dormancy
  - ETWS
  - Network selection enhancements

- **TD-SCDMA**
  - CDMA/HSDPA/HSUPA baseband
  - TD-SCDMA Bands 34, 39 & 40 and Quad band GSM/EDGE
  - Circuit-switched voice and data; packet-switched data
  - 384/384Kbps class in UL/DL for TD-SCDMA
  - TD-HSDPA: 2.8Mbps DL (Cat.14)
  - TD-HSUPA: 2.2Mbps UL (Cat.6)
  - F8/F9 ciphering/integrity protection

- **Radio interface and baseband front-end**
  - High dynamic range delta-sigma ADC converts the downlink analog I and Q signals to digital baseband.
  - 10-bit D/A converter for Automatic Power Control (APC)
  - Programmable radio Rx filter with adaptive gain control
  - Dedicated Rx filter for FB acquisition
  - Baseband Parallel Interface (BPI) with programmable driving strength
  - Supports multi-band

- **GSM modem and voice CODEC**
  - Dial tone generation
  - Noise reduction
  - Echo suppression
  - Advanced side-tone oscillation reduction
  - Digital side-tone generator with programmable gain
  - 2 programmable acoustic compensation filters
  - GSM quad vocoders for adaptive multi-rate (AMR), enhanced full rate (EFR), full rate (FR) and half rate (HR)
  - GSM channel coding, equalization and A5/1, A5/2 and A5/3 ciphering
  - GPRS GEA1, GEA2 and GEA3 ciphering
  - Programmable GSM/GPRS/EDGE modem
  - Packet switched data with CS1/CS2/CS3/CS4 coding schemes
  - GSM circuit switch data
  - GPRS/EDGE Class 12
  - Supports SAIC (Single Antenna Interference Cancellation) technology
  - VAMOS (Voice services over Adaptive Multi-user channels on One Slot) technology in R9 spec

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- **CDMA2000 modem interfaces**
  - Supports CDMA2000 1xRTT (releases 0) and CDMA2000 HRPD/1xEV-DO Revision 0 and A
  - Supports maximum 1x data rates of 153.6kbps for forward and reverse links and DO data rates of 3.1Mbps for forward link and 1.8Mbps for reverse link
  - Hybrid operation between 1x and HRPD
  - Simultaneous Hybrid Dual Receiver (SHDR) support
  - Supports 1x Diversity
  - Supports SRLTE

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1.4 Connectivity Features

MT6757 includes four wireless connectivity functions:

- WLAN
- Bluetooth
- GPS
- FM Receiver

The RF parts of those four blocks are placed on chip MT6625. With four advanced radio technologies integrated on one chip, MT6757/MT6625 is the best and most convenient connectivity solution in the industry, implementing advanced and sophisticated Radio Coexistence algorithms and hardware mechanisms. It supports single antenna sharing among 2.4GHz Bluetooth, 2.4GHz/5GHz WLAN and 1.575 GHz for GPS. The enhanced overall quality is achieved for simultaneous voice, data and audio/video transmission on mobile phones and Media Tablets. The small footprint with low-power consumption greatly reduces PCB layout resource. MT6757 also supports 802.11ac WLAN in advanced assorted with MT6630.

- **Supports integrated Wi-Fi/Bluetooth/GPS**
  - Single antenna for Bluetooth and WLAN/GPS/Bluetooth
  - Self calibration
  - Single TCXO and TMS for GPS, BT and WLAN
  - Best-in-class current consumption performance
  - Intelligent BT/WLAN coexistence scheme that goes beyond PTA signaling (e.g. transmit window and duration that take into account protocol exchange sequence, frequency, etc.)

- **Wi-Fi**
  - Dual-band (2.4GHz/5GHz) single stream 802.11 a/b/g/n MAC/BB/RF
  - 802.11 d/h/k compliant
  - Security: WFA WPA/WPA2 personal, WPS2.0, WAPI (hardware)
  - QoS: WFA WMM, WMM PS
  - 802.11n optional features: STBC, A-MPDU, Blk-Ack, RIFS, MCS Feedback, 20/40MHz coexistence (PCO), unscheduled PSMP
  - Supports 802.11w protected managed frames
  - Supports Wi-Fi Direct (WFA P-2-P standard) and Wi-Fi Miracast (Wi-Fi Display)
  - Supports Wi-Fi HotSpot 2.0
  - Integrated 2.4GHz PA with max. 19dBm CCK output power and 5GHz PA with max. 17dBm OFDM 54Mbps output power
  - Typical Rx sensitivity with companion chip modem: -75dBm at 11g 54Mbps mode and -75.5dBm at 11a 54Mbps mode
  - Per packet TX power control

- **Bluetooth**
  - Bluetooth specification v2.1+EDR
  - Bluetooth specification 3.0+HS compliance
  - Bluetooth v4.0 Low Energy (LE)
  - Integrated PA with 6dBm (class 1) transmit power
  - Typical Rx sensitivity with companion chip modem: GFSK -92.5dBm, DQPSK -91.5dBm, 8-DPSK -86dBm
  - Best-in-class BT/Wi-Fi coexistence performance
  - Up to 4 piconets simultaneously with background inquiry/page scan
  - Supports Scatternet
  - Packet Loss Concealment (PLC) function for better voice quality

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- Low-power scan function to reduce power consumption in scan modes

- **GPS**
  - Supports dual-band reception concurrently
    - GPS/Galileo only (GPS only)
    - GPS/Galileo - GLONASS (G+G)
    - GPS/Beidou (G+B)
  - Supports SBAS (Satellite-Based Augmentation Systems): WAAS/MSAS/EGNOS/GAGAN
  - Best-in-class sensitivity performance
    - -165 dBm tracking sensitivity
    - -163 dBm hot start sensitivity
    - -148 dBm cold start sensitivity
    - -151 dBm warm start sensitivity
  - AGPS sensitivity is 6dB design margin over 3GPP
  - Full A-GPS capability (E911/SUPL/EPO/HotStill)
  - Active interference cancellation for up to 12 in-band tones
  - Supports both TCXO and TMS (Thermister Crystal) clock source
  - 5Hz update rate

- **FM**
  - 65-108MHz with 50kHz step
  - RDS/RBDS
  - Digital stereo demodulator
  - Simplified digital audio interface (I2S)
  - Stereo noise reduction
  - Audio sensitivity 2dBμVemf (SINAD=26dB)
  - Audio SINAD 60dB
  - Anti-jamming
  - Integrated short antenna

- **WBT IPD**
  - Integrated matching network, balance band-pass filter, GPS-WBT diplexer
  - Fully integrated in one IPD die
  - Single and dual antenna operation

- **GPS IPD**
  - Integrated high-pass type matching network and 5th-order ellipse low-pass filter
  - Fully integrated in one IPD die
  - Single and dual antenna operation

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1.5 Multimedia Features

- **Display**
  - Portrait panel resolution up to FHD (1,920*1,080)
  - MIPI DSI interface (4 data lanes)
  - MiraVisionTM for picture quality enhancement
  - Embedded LCD gamma correction
  - True colors
  - 12 overlay layers with per-pixel alpha channel and gamma table
  - Spatial and temporal dithering
  - Side-by-side format output to stereo 3D panel in both portrait and landscape modes
  - Color enhancement
  - Adaptive contrast enhancement
  - Image/video/graphic sharpness enhancement
  - Dynamic backlight scaling
  - Wide gamut

- **Graphics**
  - OpenGL ES 3.1/3.0/2.0/1.1 3D graphic accelerator capable of processing 213M tri/sec and 1,700M pixel/sec @ 900MHz
  - OpenCL 1.2/1.1
  - Microsoft Windows compliant DirectX 11.1

- **Image**
  - Integrated image signal processor supports 21MP@30fps.
  - Electronic image stabilization
  - Video stabilization
  - Preference color adjustment
  - Noise reduction
  - Multiple frame noise reduction for image capture
  - Temporal noise reduction for video recording
  - Lens shading correction
  - Auto sensor defect pixel correction
  - Supports AE/AWB/AF
  - Edge enhancement (sharpness)
  - Face detection and visual tracking
  - Video face beautification
  - Zero shutter delay image capture
  - Captures full size image when recording video (up to 21M sensors)
  - 2 MIPI CSI-2 high-speed camera serial interfaces; both are 4 data lane
  - PIP (picture in picture), [13MP + 13MP]@24fps
  - Hardware JPEG encoder: Baseline encoding with 160M pixel/sec Continuous shot with 128M pixel/sec
  - Supports YUV422/YUV420 color format and EXIF/JFIF format

- **Video**
  - HEVC decoder 1080p @ 30fps/40Mbps
  - HEVC decoder 4K @ 30fps/10Mbps
  - H.264 decoder: Baseline 1080p @ 30fps/40Mbps
  - H.264 decoder: Main/high profile 1080p @30fps/40Mbps
  - H.264 decoder: 4K @30fps/24Mbps
  - Sorenson H.263/H.263 decoder: 1080p @ 30fps/40Mbps
  - MPEG-4 SP/ASP decoder: 1080p @ 30fps/40Mbps
  - DIVX4/DIVX5/DIVX6/DIVX HD/XVID decoder: 1080p @ 30fps/40Mbps
  - MPEG2 decoder 1080p @ 30fps/40Mbps
  - MPEG-4 encoder: Simple profile 720p @ 30fps
  - H.263 encoder: Simple profile 720p @ 30fps
  - H.264 encoder: High profile 1080p @ 30fps
  - H.264 encoder: High profile 4K @ 30fps
  –

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- HEVC encoder: Main profile 720p @ 30fps

- **Audio**
  - Audio content sampling rates supported: 8kHz to 192kHz
  - Audio content sample formats supported: 16-bit/24-bit, Mono/Stereo
  - Interfaces supported: I2S, PCM
  - External CODEC I2S interface supports 16-bit/24-bit, Mono/Stereo, 8kHz to 192kHz (Slave mode) , 8kHz to 48kHz (Master mode).
  - 4-band IIR compensation filter to enhance loudspeaker responses
  - Proprietary audio post-processing technologies: BesLoudness (MB-DRC), BesSurround, Android built-in post processing
  - Audio encoding: AMR-NB, AMR-WB, AAC, OGG, ADPCM
  - Audio decoding: WAV, MP3, MP2, AAC, AMR-NB, AMR-WB, MIDI, Vorbis, APE, AAC-plus v1, AAC-plus v2, FLAC, WMA, ADPCM

- **Speech**
  - Speech codec (FR, HR, EFR, AMR FR, AMR HR and Wide-Band AMR)
  - CTM
  - Noise reduction
  - Noise suppression
  - Noise cancellation
  - Dual-MIC noise cancellation
  - Echo cancellation
  - Echo suppression
  - Dual-MIC voice tracking
  - Dual-MIC sound recording w/o Wind Noise Rejection
  - MagiLoudness (enhances the voice clarity based on near end environment noise)
  - MagiClarity (maximizes loudness while controlling the maximum receiver output power; feed-forward receiver protection)
  - Compensation filter and digital gain for both uplink and downlink paths

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1.6 General Description

MediaTek's MT6757 is a highly integrated LTE/LTE-A System-on-Chip (SoC) which incorporates advanced features, e.g. LTE cat.6, Octa HMP cores, 3D graphics (OpenGL|ES 3.1), 20M camera ISP, LPDDR3-1866/ LPDDR4-3200, FHD display and 1080p video codec. MT6757 helps phone manufacturers build high-performance LTE/LTE-A smart phones with PC-like browser, 3D gaming and cinema class home entertainment experiences.

The World-leading Technology!
Based on MediaTek's world-leading mobile chip SoC architecture with advanced 16nm process, MT6757 is the brand-new generation smart phone SoC integrating MediaTek LTE-A modem, Octa-core ARM® Cortex-A53 MPCore™, 3D graphics and high-definition 1080p video decoder.

Rich in Features, High-Value Product!
To enrich the camera features, MT6757 equips a 20M camera ISP with advanced features, e.g. auto focus, electrical stabilization, auto sensor defect pixel correction, continuous video AF, face detection, face beautify, burst shot, optical zoom, panorama view, picture in picture, video in video and video face beautification.

Incredible Browser Experience!
The powerful CPU architecture with NEON multimedia processing engine brings PC-like browser experiences while keeping low standby power. GPU supporting OpenGL|ES 3.1 also provides you with excellent multimedia experiences.

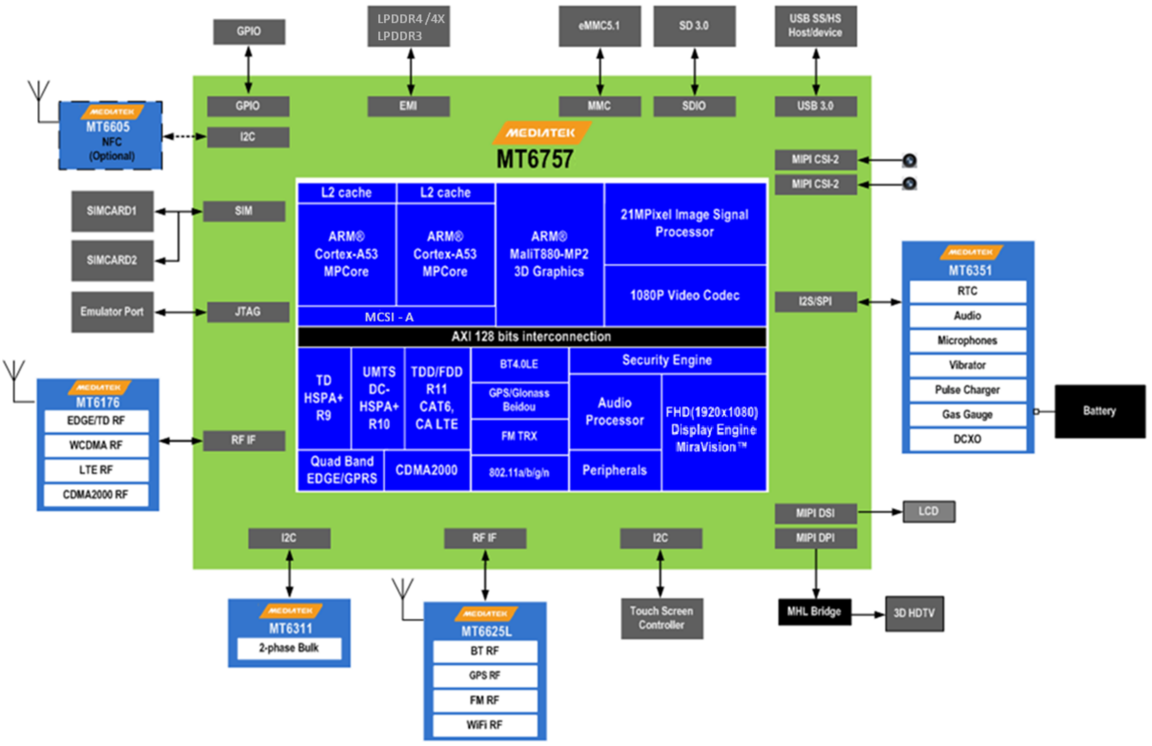

Figure 1-2. Block diagram of MT6757

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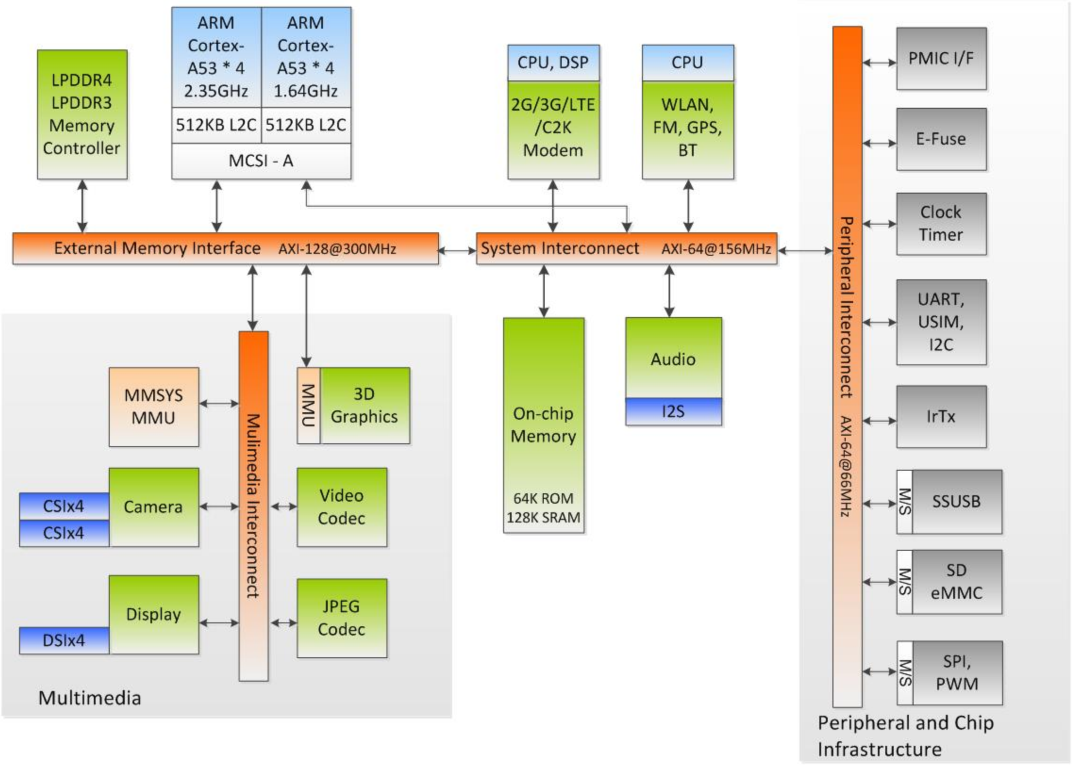

Figure 1-3. Bus structure of MT6757

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2 Product Description

2.1 Pin Description

2.1.1 Ball Map View

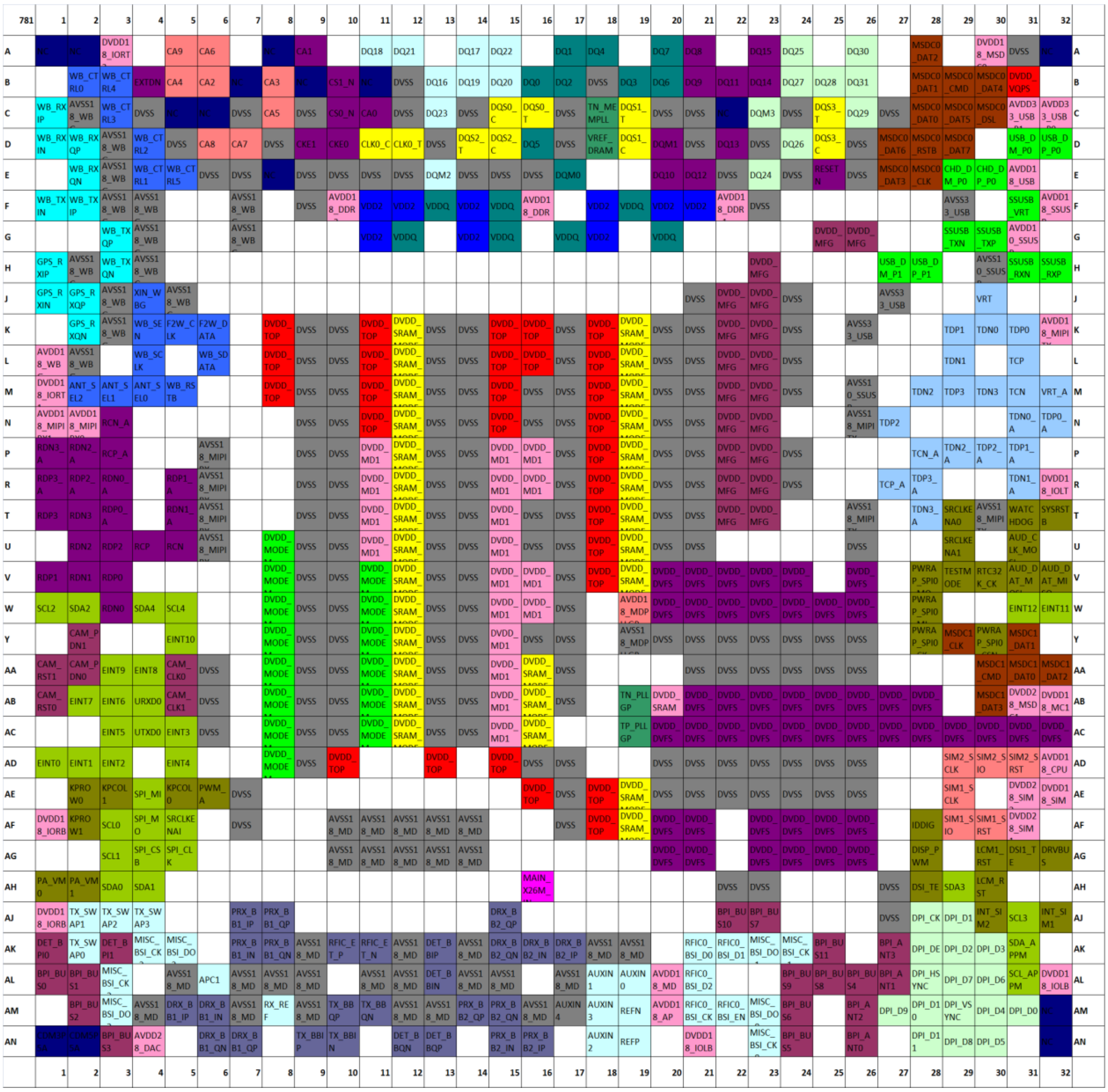

Figure 2-1. LPDDR3 ball map view

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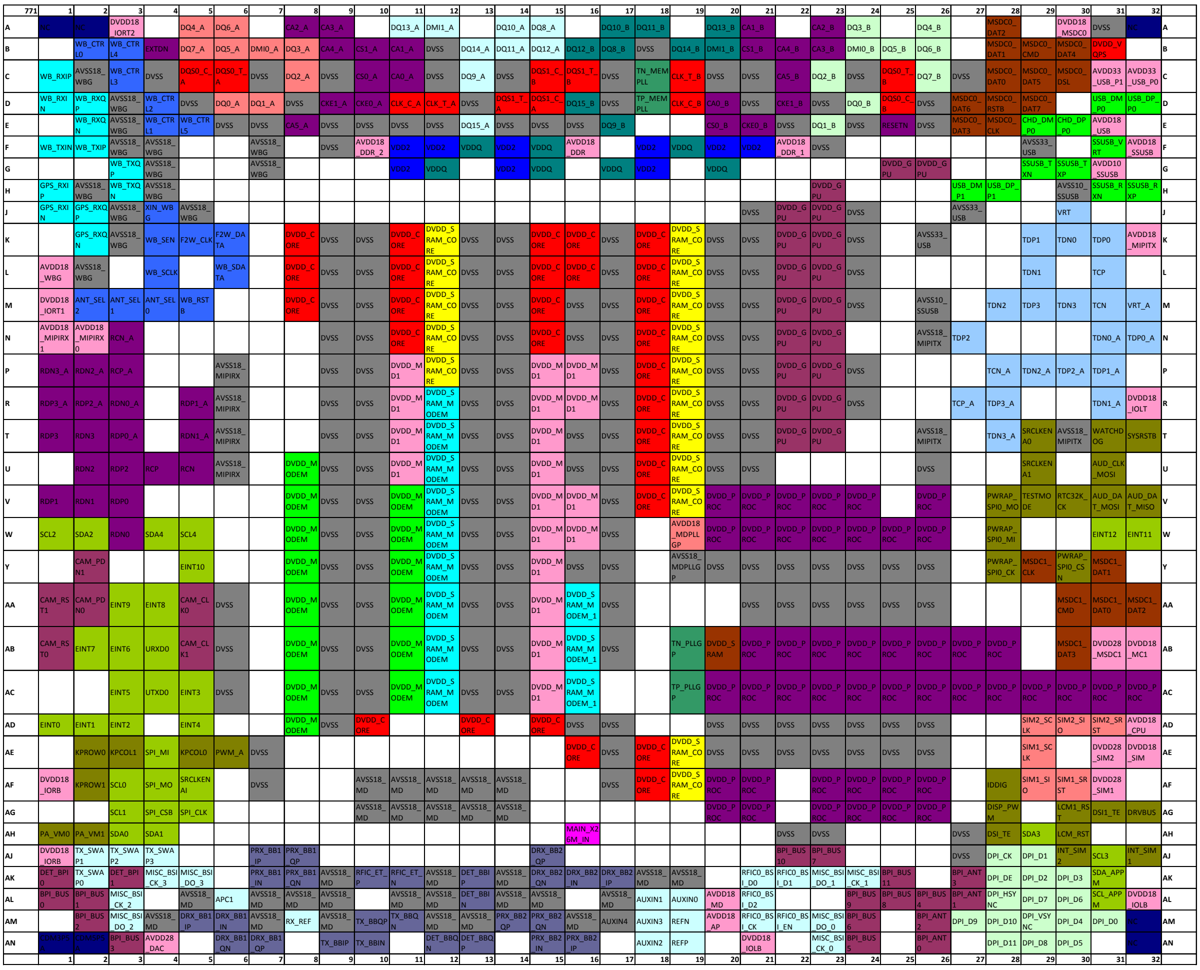

Figure 2-2. LPDDR4 ball map view

2.1.2 Pin Coordinate

Table 2-1. Pin coordinate

Ball Loc.	Ball name	Ball Loc.	Ball name	Ball Loc.	Ball name
A1	NC	M10	DVSS	AB19	TN_PLLGP
A2	NC	M11	DVDD_CORE	AB20	DVDD_SRAM
A3	DVDD18_IORT2	M12	DVDD_SRAM_CORE	AB21	DVDD_PROC
A5	DQ4_A	M13	DVSS	AB22	DVDD_PROC
A6	DQ6_A	M14	DVSS	AB23	DVDD_PROC
A8	CA2_A	M15	DVDD_CORE	AB24	DVDD_PROC
A9	CA3_A	M16	DVSS	AB25	DVDD_PROC
A11	DQ13_A	M17	DVSS	AB26	DVDD_PROC
A12	DMI1_A	M18	DVDD_CORE	AB27	DVDD_PROC
A14	DQ10_A	M19	DVDD_SRAM_CORE	AB28	DVDD_PROC

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Ball Loc.	Ball name	Ball Loc.	Ball name	Ball Loc.	Ball name
A15	DQ8_A	M20	DVSS	AB30	MSDC1_DAT3
A17	DQ10_B	M21	DVSS	AB31	DVDD28_MSDC1
A18	DQ11_B	M22	DVDD_GPU	AB32	DVDD18_MC1
A20	DQ13_B	M23	DVDD_GPU	AC3	EINT5
A21	CA1_B	M24	DVSS	AC4	UTXD0
A23	CA2_B	M26	AVSS10_SSUSB	AC5	EINT3
A24	DQ3_B	M28	TDN2	AC6	DVSS
A26	DQ4_B	M29	TDP3	AC8	DVDD_MODEM
A28	MSDC0_DAT2	M30	TDN3	AC9	DVSS
A30	DVDD18_MSDC0	M31	TCN	AC10	DVSS
A31	DVSS	M32	VRT_A	AC11	DVDD_MODEM
A32	NC	N1	AVDD18_MIPIRX1	AC12	DVDD_SRAM_MODEM
B2	WB_CTRL0	N2	AVDD18_MIPIRX0	AC13	DVSS
B3	WB_CTRL4	N3	RCN_A	AC14	DVSS
B4	EXTDN	N9	DVSS	AC15	DVDD_MD1
B5	DQ7_A	N10	DVSS	AC16	DVDD_SRAM_MODEM_1
B6	DQ5_A	N11	DVDD_CORE	AC19	TP_PLLGP
B7	DMI0_A	N12	DVDD_SRAM_CORE	AC20	DVDD_PROC
B8	DQ3_A	N13	DVSS	AC21	DVDD_PROC
B9	CA4_A	N14	DVSS	AC22	DVDD_PROC
B10	CS1_A	N15	DVDD_CORE	AC23	DVDD_PROC
B11	CA1_A	N16	DVSS	AC24	DVDD_PROC
B12	DVSS	N17	DVSS	AC25	DVDD_PROC
B13	DQ14_A	N18	DVDD_CORE	AC26	DVDD_PROC
B14	DQ11_A	N19	DVDD_SRAM_CORE	AC27	DVDD_PROC
B15	DQ12_A	N20	DVSS	AC28	DVDD_PROC
B16	DQ12_B	N21	DVSS	AC29	DVDD_PROC
B17	DQ8_B	N22	DVDD_GPU	AC30	DVDD_PROC
B18	DVSS	N23	DVDD_GPU	AC31	DVDD_PROC
B19	DQ14_B	N26	AVSS18_MIPITX	AC32	DVDD_PROC
B20	DMI1_B	N27	TDP2	AD1	EINT0
B21	CS1_B	N31	TDN0_A	AD2	EINT1
B22	CA4_B	N32	TDP0_A	AD3	EINT2
B23	CA3_B	P1	RDN3_A	AD5	EINT4
B24	DMI0_B	P2	RDN2_A	AD8	DVDD_MODEM
B25	DQ5_B	P3	RCP_A	AD9	DVSS
B26	DQ6_B	P6	AVSS18_MIPIRX	AD10	DVDD_CORE
B28	MSDC0_DAT1	P9	DVSS	AD13	DVDD_CORE
B29	MSDC0_CMD	P10	DVSS	AD15	DVDD_CORE
B30	MSDC0_DAT4	P11	DVDD_MD1	AD16	DVSS
B31	DVDD_VQPS	P12	DVDD_SRAM_CORE	AD17	DVSS

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Ball Loc.	Ball name	Ball Loc.	Ball name	Ball Loc.	Ball name
C1	WB_RXIP	P13	DVSS	AD20	DVSS
C2	AVSS18_WBG	P14	DVSS	AD21	DVSS
C3	WB_CTRL3	P15	DVDD_MD1	AD22	DVSS
C4	DVSS	P16	DVDD_MD1	AD23	DVSS
C5	DQS0_C_A	P17	DVSS	AD24	DVSS
C6	DQS0_T_A	P18	DVDD_CORE	AD25	DVSS
C7	DVSS	P19	DVDD_SRAM_CORE	AD26	DVSS
C8	DQ2_A	P20	DVSS	AD29	SIM2_SCLK
C9	DVSS	P21	DVSS	AD30	SIM2_SIO
C10	CS0_A	P22	DVDD_GPU	AD31	SIM2_SRST
C11	CA0_A	P23	DVDD_GPU	AD32	AVDD18_CPU
C12	DVSS	P24	DVSS	AE2	KPROW0
C13	DQ9_A	P28	TCN_A	AE3	KPCOL1
C14	DVSS	P29	TDN2_A	AE4	SPI_MI
C15	DQS1_C_B	P30	TDP2_A	AE5	KPCOL0
C16	DQS1_T_B	P31	TDP1_A	AE6	PWM_A
C17	DVSS	R1	RDP3_A	AE7	DVSS
C18	TN_MEMPLL	R2	RDP2_A	AE16	DVDD_CORE
C19	CLK_T_B	R3	RDN0_A	AE17	DVSS
C20	DVSS	R5	RDP1_A	AE18	DVDD_CORE
C21	DVSS	R6	AVSS18_MIPIRX	AE19	DVDD_SRAM_CORE
C22	CA5_B	R9	DVSS	AE20	DVSS
C23	DQ2_B	R10	DVSS	AE21	DVSS
C24	DVSS	R11	DVDD_MD1	AE22	DVSS
C25	DQS0_T_B	R12	DVDD_SRAM_MODEM	AE23	DVSS
C26	DQ7_B	R13	DVSS	AE24	DVSS
C27	DVSS	R14	DVSS	AE25	DVSS
C28	MSDC0_DAT0	R15	DVDD_MD1	AE26	DVSS
C29	MSDC0_DAT5	R16	DVDD_MD1	AE29	SIM1_SCLK
C30	MSDC0_DSL	R17	DVSS	AE31	DVDD28_SIM2
C31	AVDD33_USB_P1	R18	DVDD_CORE	AE32	DVDD18_SIM
C32	AVDD33_USB_P0	R19	DVDD_SRAM_CORE	AF1	DVDD18_IORB
D1	WB_RXIN	R20	DVSS	AF2	KPROW1
D2	WB_RXQP	R21	DVSS	AF3	SCL0
D3	AVSS18_WBG	R22	DVDD_GPU	AF4	SPI_MO
D4	WB_CTRL2	R23	DVDD_GPU	AF5	SRCLKENAI
D5	DVSS	R24	DVSS	AF7	DVSS
D6	DQ0_A	R27	TCP_A	AF10	AVSS18_MD
D7	DQ1_A	R28	TDP3_A	AF11	AVSS18_MD
D8	DVSS	R31	TDN1_A	AF12	AVSS18_MD
D9	CKE1_A	R32	DVDD18_IOLT	AF13	AVSS18_MD

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Ball Loc.	Ball name	Ball Loc.	Ball name	Ball Loc.	Ball name
D10	CKE0_A	T1	RDP3	AF14	AVSS18_MD
D11	CLK_C_A	T2	RDN3	AF17	DVSS
D12	CLK_T_A	T3	RDP0_A	AF18	DVDD_CORE
D13	DVSS	T5	RDN1_A	AF19	DVDD_SRAM_CORE
D14	DQS1_T_A	T6	AVSS18_MIPIRX	AF20	DVDD_PROC
D15	DQS1_C_A	T9	DVSS	AF21	DVDD_PROC
D16	DQ15_B	T10	DVSS	AF23	DVDD_PROC
D17	DVSS	T11	DVDD_MD1	AF24	DVDD_PROC
D18	TP_MEMPLL	T12	DVDD_SRAM_MODEM	AF25	DVDD_PROC
D19	CLK_C_B	T13	DVSS	AF26	DVDD_PROC
D20	CA0_B	T14	DVSS	AF28	IDDIG
D21	DVSS	T15	DVDD_MD1	AF29	SIM1_SIO
D22	CKE1_B	T16	DVSS	AF30	SIM1_SRST
D23	DVSS	T17	DVSS	AF31	DVDD28_SIM1
D24	DQ0_B	T18	DVDD_CORE	AG3	SCL1
D25	DQS0_C_B	T19	DVDD_SRAM_CORE	AG4	SPI_CSB
D26	DVSS	T20	DVSS	AG5	SPI_CLK
D27	MSDC0_DAT6	T21	DVSS	AG10	AVSS18_MD
D28	MSDC0_RSTB	T22	DVDD_GPU	AG11	AVSS18_MD
D29	MSDC0_DAT7	T23	DVDD_GPU	AG12	AVSS18_MD
D31	USB_DM_P0	T26	AVSS18_MIPITX	AG13	AVSS18_MD
D32	USB_DP_P0	T28	TDN3_A	AG14	AVSS18_MD
E2	WB_RXQN	T29	SRCLKENA0	AG20	DVDD_PROC
E3	AVSS18_WBG	T30	AVSS18_MIPITX	AG21	DVDD_PROC
E4	WB_CTRL1	T31	WATCHDOG	AG23	DVDD_PROC
E5	WB_CTRL5	T32	SYSRSTB	AG24	DVDD_PROC
E6	DVSS	U2	RDN2	AG25	DVDD_PROC
E7	DVSS	U3	RDP2	AG26	DVDD_PROC
E8	CA5_A	U4	RCP	AG28	DISP_PWM
E9	DVSS	U5	RCN	AG30	LCM1_RST
E10	DVSS	U6	AVSS18_MIPIRX	AG31	DSI1_TE
E11	DVSS	U8	DVDD_MODEM	AG32	DRVBUS
E12	DVSS	U9	DVSS	AH1	PA_VM0
E13	DQ15_A	U10	DVSS	AH2	PA_VM1
E14	DVSS	U11	DVDD_MD1	AH3	SDA0
E15	DVSS	U12	DVDD_SRAM_MODEM	AH4	SDA1
E16	DVSS	U13	DVSS	AH16	MAIN_X26M_IN
E17	DQ9_B	U14	DVSS	AH22	DVSS
E20	CS0_B	U15	DVDD_MD1	AH23	DVSS
E21	CKE0_B	U16	DVSS	AH27	DVSS
E22	DVSS	U17	DVSS	AH28	DSI_TE

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Ball Loc.	Ball name	Ball Loc.	Ball name	Ball Loc.	Ball name
E23	DQ1_B	U18	DVDD_CORE	AH29	SDA3
E24	DVSS	U19	DVDD_SRAM_CORE	AH30	LCM_RST
E25	RESETN	U20	DVSS	AJ1	DVDD18_IORB
E26	DVSS	U21	DVSS	AJ2	TX_SWAP1
E27	MSDC0_DAT3	U26	DVSS	AJ3	TX_SWAP2
E28	MSDC0_CLK	U29	SRCLKENA1	AJ4	TX_SWAP3
E29	CHD_DM_P0	U31	AUD_CLK_MOSI	AJ7	PRX_BB1_IP
E30	CHD_DP_P0	V1	RDP1	AJ8	PRX_BB1_QP
E31	AVDD18_USB	V2	RDN1	AJ15	DRX_BB2_QP
F1	WB_TXIN	V3	RDP0	AJ22	BPI_BUS10
F2	WB_TXIP	V8	DVDD_MODEM	AJ23	BPI_BUS7
F3	AVSS18_WBG	V9	DVSS	AJ27	DVSS
F4	AVSS18_WBG	V10	DVSS	AJ28	DPI_CK
F7	AVSS18_WBG	V11	DVDD_MODEM	AJ29	DPI_D1
F9	DVSS	V12	DVDD_SRAM_MODEM	AJ30	INT_SIM2
F10	AVDD18_DDR_2	V13	DVSS	AJ31	SCL3
F11	VDD2	V14	DVSS	AJ32	INT_SIM1
F12	VDD2	V15	DVDD_MD1	AK1	DET_BPI0
F13	VDDQ	V16	DVDD_MD1	AK2	TX_SWAP0
F14	VDD2	V17	DVSS	AK3	DET_BPI1
F15	VDDQ	V18	DVDD_CORE	AK4	MISC_BSI_CK_3
F16	AVDD18_DDR	V19	DVDD_SRAM_CORE	AK5	MISC_BSI_DO_3
F18	VDD2	V20	DVDD_PROC	AK7	PRX_BB1_IN
F19	VDDQ	V21	DVDD_PROC	AK8	PRX_BB1_QN
F20	VDD2	V22	DVDD_PROC	AK9	AVSS18_MD
F21	VDD2	V23	DVDD_PROC	AK10	RFIC_ET_P
F22	AVDD18_DDR_1	V24	DVDD_PROC	AK11	RFIC_ET_N
F23	DVSS	V26	DVDD_PROC	AK12	AVSS18_MD
F29	AVSS33_USB	V28	PWRAP_SPI0_MO	AK13	DET_BBIP
F31	SSUSB_VRT	V29	TESTMODE	AK14	AVSS18_MD
F32	AVDD18_SSUSB	V30	RTC32K_CK	AK15	DRX_BB2_QN
G3	WB_TXQP	V31	AUD_DAT_MOSI	AK16	DRX_BB2_IN
G4	AVSS18_WBG	V32	AUD_DAT_MISO	AK17	DRX_BB2_IP
G7	AVSS18_WBG	W1	SCL2	AK18	AVSS18_MD
G11	VDD2	W2	SDA2	AK19	AVSS18_MD
G12	VDDQ	W3	RDN0	AK21	RFIC0_BSI_D0
G14	VDD2	W4	SDA4	AK22	RFIC0_BSI_D1
G15	VDDQ	W5	SCL4	AK23	MISC_BSI_DO_1
G17	VDDQ	W8	DVDD_MODEM	AK24	MISC_BSI_CK_1
G18	VDD2	W9	DVSS	AK25	BPI_BUS11
G20	VDDQ	W10	DVSS	AK27	BPI_ANT3

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Ball Loc.	Ball name	Ball Loc.	Ball name	Ball Loc.	Ball name
G25	DVDD_GPU	W11	DVDD_MODEM	AK28	DPI_DE
G26	DVDD_GPU	W12	DVDD_SRAM_MODEM	AK29	DPI_D2
G29	SSUSB_TXN	W13	DVSS	AK30	DPI_D3
G30	SSUSB_TXP	W14	DVSS	AK31	SDA_APPM
G31	AVDD10_SSUSB	W15	DVDD_MD1	AL1	BPI_BUS0
H1	GPS_RXIP	W16	DVDD_MD1	AL2	BPI_BUS1
H2	AVSS18_WBG	W17	DVSS	AL3	MISC_BSI_CK_2
H3	WB_TXQN	W19	AVDD18_MDPLLGP	AL5	AVSS18_MD
H4	AVSS18_WBG	W20	DVDD_PROC	AL6	APC1
H23	DVDD_GPU	W21	DVDD_PROC	AL7	AVSS18_MD
H27	USB_DM_P1	W22	DVDD_PROC	AL8	AVSS18_MD
H28	USB_DP_P1	W23	DVDD_PROC	AL9	AVSS18_MD
H30	AVSS10_SSUSB	W24	DVDD_PROC	AL11	AVSS18_MD
H31	SSUSB_RXN	W25	DVDD_PROC	AL12	AVSS18_MD
H32	SSUSB_RXP	W26	DVDD_PROC	AL13	DET_BBIN
J1	GPS_RXIN	W28	PWRAP_SPI0_MI	AL14	AVSS18_MD
J2	GPS_RXQP	W31	EINT12	AL15	AVSS18_MD
J3	AVSS18_WBG	W32	EINT11	AL17	AVSS18_MD
J4	XIN_WBG	Y2	CAM_PDN1	AL18	AUXIN1
J5	AVSS18_WBG	Y5	EINT10	AL19	AUXIN0
J21	DVSS	Y8	DVDD_MODEM	AL20	AVDD18_MD
J22	DVDD_GPU	Y9	DVSS	AL21	RFIC0_BSI_D2
J23	DVDD_GPU	Y10	DVSS	AL24	BPI_BUS9
J24	DVSS	Y11	DVDD_MODEM	AL25	BPI_BUS8
J27	AVSS33_USB	Y12	DVDD_SRAM_MODEM	AL26	BPI_BUS4
J30	VRT	Y13	DVSS	AL27	BPI_ANT1
K2	GPS_RXQN	Y14	DVSS	AL28	DPI_HSYNC
K3	AVSS18_WBG	Y15	DVDD_MD1	AL29	DPI_D7
K4	WB_SEN	Y16	DVSS	AL30	DPI_D6
K5	F2W_CLK	Y17	DVSS	AL31	SCL_APPM
K6	F2W_DATA	Y19	AVSS18_MDPLLGP	AL32	DVDD18_IOLB
K8	DVDD_CORE	Y20	DVSS	AM2	BPI_BUS2
K9	DVSS	Y21	DVSS	AM3	MISC_BSI_DO_2
K10	DVSS	Y22	DVSS	AM4	AVSS18_MD
K11	DVDD_CORE	Y23	DVSS	AM5	DRX_BB1_IP
K12	DVDD_SRAM_CORE	Y24	DVSS	AM6	DRX_BB1_IN
K13	DVSS	Y25	DVSS	AM7	AVSS18_MD
K14	DVSS	Y26	DVSS	AM8	RX_REF
K15	DVDD_CORE	Y28	PWRAP_SPI0_CK	AM9	AVSS18_MD
K16	DVDD_CORE	Y29	MSDC1_CLK	AM10	TX_BBQP
K17	DVSS	Y30	PWRAP_SPI0_CSN	AM11	TX_BBQN

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Ball Loc.	Ball name	Ball Loc.	Ball name	Ball Loc.	Ball name
K18	DVDD_CORE	Y31	MSDC1_DAT1	AM12	AVSS18_MD
K19	DVDD_SRAM_CORE	AA1	CAM_RST1	AM13	AVSS18_MD
K20	DVSS	AA2	CAM_PDN0	AM14	PRX_BB2_QP
K21	DVSS	AA3	EINT9	AM15	PRX_BB2_QN
K22	DVDD_GPU	AA4	EINT8	AM16	AVSS18_MD
K23	DVDD_GPU	AA5	CAM_CLK0	AM17	AUXIN4
K24	DVSS	AA6	DVSS	AM18	AUXIN3
K26	AVSS33_USB	AA8	DVDD_MODEM	AM19	REFN
K29	TDP1	AA9	DVSS	AM20	AVDD18_AP
K30	TDN0	AA10	DVSS	AM21	RFIC0_BSI_CK
K31	TDP0	AA11	DVDD_MODEM	AM22	RFIC0_BSI_EN
K32	AVDD18_MIPITX	AA12	DVDD_SRAM_MODEM	AM23	MISC_BSI_DO_0
L1	AVDD18_WBG	AA13	DVSS	AM24	BPI_BUS6
L2	AVSS18_WBG	AA14	DVSS	AM26	BPI_ANT2
L4	WB_SCLK	AA15	DVDD_MD1	AM27	DPI_D9
L6	WB_SDATA	AA16	DVDD_SRAM_MODEM_1	AM28	DPI_D10
L8	DVDD_CORE	AA17	DVSS	AM29	DPI_VSYNC
L9	DVSS	AA21	DVSS	AM30	DPI_D4
L10	DVSS	AA22	DVSS	AM31	DPI_D0
L11	DVDD_CORE	AA23	DVSS	AM32	NC
L12	DVDD_SRAM_CORE	AA24	DVSS	AN1	CDM3P5A
L13	DVSS	AA25	DVSS	AN2	CDM5P5A
L14	DVSS	AA26	DVSS	AN3	BPI_BUS3
L15	DVDD_CORE	AA30	MSDC1_CMD	AN4	AVDD28_DAC
L16	DVDD_CORE	AA31	MSDC1_DAT0	AN6	DRX_BB1_QN
L17	DVSS	AA32	MSDC1_DAT2	AN7	DRX_BB1_QP
L18	DVDD_CORE	AB1	CAM_RST0	AN9	TX_BBIP
L19	DVDD_SRAM_CORE	AB2	EINT7	AN10	TX_BBIN
L20	DVSS	AB3	EINT6	AN12	DET_BBQN
L21	DVSS	AB4	URXD0	AN13	DET_BBQP
L22	DVDD_GPU	AB5	CAM_CLK1	AN15	PRX_BB2_IN
L23	DVDD_GPU	AB6	DVSS	AN16	PRX_BB2_IP
L24	DVSS	AB8	DVDD_MODEM	AN18	AUXIN2
L29	TDN1	AB9	DVSS	AN19	REFP
L31	TCP	AB10	DVSS	AN21	DVDD18_IOLB
M1	DVDD18_IORT1	AB11	DVDD_MODEM	AN23	MISC_BSI_CK_0
M2	ANT_SEL2	AB12	DVDD_SRAM_MODEM	AN24	BPI_BUS5
M3	ANT_SEL1	AB13	DVSS	AN26	BPI_ANT0
M4	ANT_SEL0	AB14	DVSS	AN28	DPI_D11
M5	WB_RSTB	AB15	DVDD_MD1	AN29	DPI_D8
M8	DVDD_CORE	AB16	DVDD_SRAM_MODEM_1	AN30	DPI_D5

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Ball Loc.	Ball name	Ball Loc.	Ball name	Ball Loc.	Ball name
M9	DVSS	AB17	DVSS	AN32	NC

2.1.3 Detailed Pin Description

Table 2-2. Acronym for pin type

Abbreviation	Description
AI	Analog input
AO	Analog output
AIO	Analog bi-direction
DI	Digital input
DO	Digital output
DIO	Digital bi-direction
P	Power
G	Ground

Table 2-3. Detailed pin description (using LPDDR4)

Pin name	Pin #	Type	Description	Power domain
SYSTEM				
SYSRSTB	T32	DIO	System reset input	DVDD18_IOLT
WATCHDOG	T31	DO	Watchdog reset output	DVDD18_IOLT
TESTMODE	V29	DIO	Test mode	DVDD18_IOLT
RTC32K_CK	V30	DIO	RTC 32K input	DVDD18_IOLT
SRCLKENA0	T29	DIO		DVDD18_IOLT
SRCLKENA1	U29	DIO		DVDD18_IOLT
SRCLKENAI	AF5	DIO		DVDD18_IORB
PMIC				
PWRAP_SPI0_MO	V28	DIO	PMIC SPI control interface	DVDD18_IOLT
PWRAP_SPI0_MI	W28	DIO	PMIC SPI control interface	DVDD18_IOLT
PWRAP_SPI0_CSN	Y30	DIO	PMIC SPI control interface	DVDD18_IOLT
PWRAP_SPI0_CK	Y28	DIO	PMIC SPI control interface	DVDD18_IOLT
AUD_CLK_MOSI	U31	DIO	PMIC audio input interface	DVDD18_IOLT
AUD_DAT_MISO	V32	DIO	PMIC audio input interface	DVDD18_IOLT
AUD_DAT_MOSI	V31	DIO	PMIC audio input interface	DVDD18_IOLT
SIM				
SIM1_SCLK	AE29	DIO	SIM1 clock, PMIC interface	DVDD28_SIM1
SIM1_SIO	AF29	DIO	SIM1 data, PMIC interface	DVDD28_SIM1
SIM1_SRST	AF30	DIO	SIM1 data, PMIC interface	DVDD28_SIM1
SIM2_SCLK	AD29	DIO	SIM2 clock, PMIC interface	DVDD28_SIM2
SIM2_SIO	AD30	DIO	SIM2 data, PMIC interface	DVDD28_SIM2

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Pin name	Pin #	Type	Description	Power domain
SIM2_SRST	AD31	DIO	SIM2 data, PMIC interface	DVDD28_SIM2
INT_SIM1	AJ32	DIO	SIM1 interrupt	DVDD18_IOLB
INT_SIM2	AJ30	DIO	SIM2 interrupt	DVDD18_IOLB
LCD				
DSI_TE	AH28	DIO	Parallel display interface tearing effect	DVDD18_IOLB
LCM_RST	AH30	DIO	Parallel display interface reset signal	DVDD18_IOLB
DPI_HSYNC	AL28	DIO	Parallel display interface HSYNC	DVDD18_IOLB
DPI_VSYNC	AM29	DIO	Parallel display interface VSYNC	DVDD18_IOLB
DPI_CK	AJ28	DIO	Parallel display interface CLK	DVDD18_IOLB
DPI_DE	AK28	DIO	Parallel display interface DE	DVDD18_IOLB
DPI_D11	AN28	DIO	Data pin 11 for DPI parallel LCD interface	DVDD18_IOLB
DPI_D10	AM28	DIO	Data pin 10 for DPI parallel LCD interface	DVDD18_IOLB
DPI_D9	AM27	DIO	Data pin 9 for DPI parallel LCD interface	DVDD18_IOLB
DPI_D8	AN29	DIO	Data pin 8 for DPI parallel LCD interface	DVDD18_IOLB
DPI_D7	AL29	DIO	Data pin 7 for DPI parallel LCD interface	DVDD18_IOLB
DPI_D6	AL30	DIO	Data pin 6 for DPI parallel LCD interface	DVDD18_IOLB
DPI_D5	AN30	DIO	Data pin 5 for DPI parallel LCD interface	DVDD18_IOLB
DPI_D4	AM30	DIO	Data pin 4 for DPI parallel LCD interface	DVDD18_IOLB
DPI_D3	AK30	DIO	Data pin 3 for DPI parallel LCD interface	DVDD18_IOLB
DPI_D2	AK29	DIO	Data pin 2 for DPI parallel LCD interface	DVDD18_IOLB
DPI_D1	AJ29	DIO	Data pin 1 for DPI parallel LCD interface	DVDD18_IOLB
DPI_D0	AM31	DIO	Data pin 0 for DPI parallel LCD interface	DVDD18_IOLB
PWM				
PWM_A	AE6	DIO	PWM_A	DVDD18_IORB
DISP_PWM	AG28	DIO	Display PWM	DVDD18_IOLB
Keypad Interface				
KPCOL0	AE5	DIO	Keypad column 0	DVDD18_IORB
KPCOL1	AE3	DIO	Keypad column 1	DVDD18_IORB
KPROW0	AE2	DIO	Keypad row 0	DVDD18_IORB
KPROW1	AF2	DIO	Keypad row 1	DVDD18_IORB
SPI				
SPI_CSB	AG4	DIO	SPI chip select	DVDD18_IORB
SPI_MI	AE4	DIO	SPI data in	DVDD18_IORB

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Pin name	Pin #	Type	Description	Power domain
SPI_MO	AF4	DIO	SPI data out	DVDD18_IORB
SPI_CLK	AG5	DIO	SPI clock	DVDD18_IORB
BPI				
BPI_BUS0	AL1	DIO	BPI_BUS0	DVDD18_IOBR
BPI_BUS1	AL2	DIO	BPI_BUS1	DVDD18_IOBR
BPI_BUS2	AM2	DIO	BPI_BUS2	DVDD18_IOBR
BPI_BUS3	AN3	DIO	BPI_BUS3	DVDD18_IOBR
BPI_BUS4	AL26	DIO	BPI_BUS4	DVDD18_IOBL
BPI_BUS5	AN24	DIO	BPI_BUS5	DVDD18_IOBL
BPI_BUS6	AM24	DIO	BPI_BUS6	DVDD18_IOBL
BPI_BUS7	AJ23	DIO	BPI_BUS7	DVDD18_IOBL
BPI_BUS8	AL25	DIO	BPI_BUS8	DVDD18_IOBL
BPI_BUS9	AL24	DIO	BPI_BUS9	DVDD18_IOBL
BPI_BUS10	AJ22	DIO	BPI_BUS10	DVDD18_IOBL
BPI_BUS11	AK25	DIO	BPI_BUS11	DVDD18_IOBL
BPI_ANT0	AN26	DIO	BPI_ANT0	DVDD18_IOBL
BPI_ANT1	AL27	DIO	BPI_ANT1	DVDD18_IOBL
BPI_ANT2	AM26	DIO	BPI_ANT2	DVDD18_IOBL
DET_BPI0	AK1	DIO	DET_BPI0	DVDD18_IOBL
DET_BPI1	AK3	DIO	DET_BPI1	DVDD18_IOBL
TX_SWAP0	AK2	DIO	TX_SWAP0	DVDD18_IOBR
TX_SWAP1	AJ2	DIO	TX_SWAP1	DVDD18_IOBR
TX_SWAP2	AJ3	DIO	TX_SWAP2	DVDD18_IOBR
TX_SWAP3	AJ4	DIO	TX_SWAP3	DVDD18_IOBR
PA_VM0	AH1	DIO	PA_VM0	DVDD18_IOBR
PA_VM1	AH2	DIO	PA_VM1	DVDD18_IOBR
BSI				
RFIC0_BSI_CK	AM21	DIO	RFIC0 BSI CLK	DVDD18_IOBL
RFIC0_BSI_D0	AK21	DIO	RFIC0 BSI DATA0	DVDD18_IOBL
RFIC0_BSI_D1	AK22	DIO	RFIC0 BSI DATA1	DVDD18_IOBL
RFIC0_BSI_D2	AL21	DIO	RFIC0 BSI DATA2	DVDD18_IOBL
RFIC0_BSI_EN	AM22	DIO	RFIC0 BSI CS	DVDD18_IOBL
MISC_BSI_DO_0	AM23	DIO	MISC_BSI_DO_0	DVDD18_IOBL
MISC_BSI_CK_0	AN23	DIO	MISC_BSI_CK_0	DVDD18_IOBL
MISC_BSI_DO_1	AK23	DIO	MISC_BSI_DO_1	DVDD18_IOBL
MISC_BSI_CK_1	AK24	DIO	MISC_BSI_CK_1	DVDD18_IOBL
MISC_BSI_DO_2	AM3	DIO	MISC_BSI_DO_2	DVDD18_IOBR
MISC_BSI_CK_2	AL3	DIO	MISC_BSI_CK_2	DVDD18_IOBR
MISC_BSI_DO_3	AK5	DIO	MISC_BSI_DO_3	DVDD18_IOBR
MISC_BSI_CK_3	AK4	DIO	MISC_BSI_CK_3	DVDD18_IOBR
MSDC1				
MSDC1_CLK	Y29	DIO	MSDC1 clock output	DVDD28_MSDC1

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Pin name	Pin #	Type	Description	Power domain
MSDC1_CMD	AA30	DIO	MSDC1 command pin	DVDD28_MSDC1
MSDC1_DAT0	AA31	DIO	MSDC1 data0 pin	DVDD28_MSDC1
MSDC1_DAT1	Y31	DIO	MSDC1 data1 pin	DVDD28_MSDC1
MSDC1_DAT2	AA32	DIO	MSDC1 data2 pin	DVDD28_MSDC1
MSDC1_DAT3	AB30	DIO	MSDC1 data3 pin	DVDD28_MSDC1
MSDC0				
MSDC0_CLK	E28	DIO	MSDC0 clock output	DVDD18_MSDC0
MSDC0_CMD	B29	DIO	MSDC0 command pin	DVDD18_MSDC0
MSDC0_DAT0	C28	DIO	MSDC0 data0 pin	DVDD18_MSDC0
MSDC0_DAT1	B28	DIO	MSDC0 data1 pin	DVDD18_MSDC0
MSDC0_DAT2	A28	DIO	MSDC0 data2 pin	DVDD18_MSDC0
MSDC0_DAT3	E27	DIO	MSDC0 data3 pin	DVDD18_MSDC0
MSDC0_DAT4	B30	DIO	MSDC0 data4 pin	DVDD18_MSDC0
MSDC0_DAT5	C29	DIO	MSDC0 data5 pin	DVDD18_MSDC0
MSDC0_DAT6	D27	DIO	MSDC0 data6 pin	DVDD18_MSDC0
MSDC0_DAT7	D29	DIO	MSDC0 data7 pin	DVDD18_MSDC0
MSDC0_DSL	C30	DIO	MSDC0 DSL pin	DVDD18_MSDC0
MSDC0_RSTB	D28	DIO	MSDC0 Reset pin	DVDD18_MSDC0
EFUSE				
DVDD_VQPS	B31	DIO	E-FUSE blowing power control	DVDD_VQPS
EMI				
DQ7_A	B5	DIO	DRAM interface	DDRV
DQ4_A	A5	DIO	DRAM interface	DDRV
DQ0_A	D6	DIO	DRAM interface	DDRV
DQ1_A	D7	DIO	DRAM interface	DDRV
DQS0_T_A	C6	DIO	DRAM interface	DDRV
DQS0_C_A	C5	DIO	DRAM interface	DDRV
DQ5_A	B6	DIO	DRAM interface	DDRV
DQ6_A	A6	DIO	DRAM interface	DDRV
DQ3_A	B8	DIO	DRAM interface	DDRV
DQ2_A	C8	DIO	DRAM interface	DDRV
DMI0_A	B7	DIO	DRAM interface	DDRV
CA5_A	E8	DIO	DRAM interface	DDRV
CKE1_A	D9	DIO	DRAM interface	DDRV
CKE0_A	D10	DIO	DRAM interface	DDRV
CS0_A	C10	DIO	DRAM interface	DDRV
CA0_A	C11	DIO	DRAM interface	DDRV
CLK_T_A	D12	DIO	DRAM interface	DDRV
CLK_C_A	D11	DIO	DRAM interface	DDRV
CA3_A	A9	DIO	DRAM interface	DDRV
CA2_A	A8	DIO	DRAM interface	DDRV
CA4_A	B9	DIO	DRAM interface	DDRV

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Pin name	Pin #	Type	Description	Power domain
CA1_A	B11	DIO	DRAM interface	DDRV
DMI1_A	A12	DIO	DRAM interface	DDRV
CS1_A	B10	DIO	DRAM interface	DDRV
DQ14_A	B13	DIO	DRAM interface	DDRV
DQ13_A	A11	DIO	DRAM interface	DDRV
DQ11_A	B14	DIO	DRAM interface	DDRV
DQ10_A	A14	DIO	DRAM interface	DDRV
DQS1_T_A	D14	DIO	DRAM interface	DDRV
DQS1_C_A	D15	DIO	DRAM interface	DDRV
DQ15_A	E13	DIO	DRAM interface	DDRV
DQ9_A	C13	DIO	DRAM interface	DDRV
DQ12_A	B15	DIO	DRAM interface	DDRV
DQ8_A	A15	DIO	DRAM interface	DDRV
TP_MEMPLL	D18	DIO	DRAM interface	DDRV
TN_MEMPLL	C18	DIO	DRAM interface	DDRV
DQ12_B	B16	DIO	DRAM interface	DDRV
DQ8_B	B17	DIO	DRAM interface	DDRV
DQ15_B	D16	DIO	DRAM interface	DDRV
DQ9_B	E17	DIO	DRAM interface	DDRV
DQS1_T_B	C16	DIO	DRAM interface	DDRV
DQS1_C_B	C15	DIO	DRAM interface	DDRV
DQ11_B	A18	DIO	DRAM interface	DDRV
DQ10_B	A17	DIO	DRAM interface	DDRV
DQ14_B	B19	DIO	DRAM interface	DDRV
DQ13_B	A20	DIO	DRAM interface	DDRV
DMI1_B	B20	DIO	DRAM interface	DDRV
CS1_B	B21	DIO	DRAM interface	DDRV
CA4_B	B22	DIO	DRAM interface	DDRV
CA1_B	A21	DIO	DRAM interface	DDRV
CA3_B	B23	DIO	DRAM interface	DDRV
CA2_B	A23	DIO	DRAM interface	DDRV
CLK_T_B	C19	DIO	DRAM interface	DDRV_CLK
CLK_C_B	D19	DIO	DRAM interface	DDRV_CLK
CS0_B	E20	DIO	DRAM interface	DDRV
CA0_B	D20	DIO	DRAM interface	DDRV
CKE1_B	D22	DIO	DRAM interface	DDRV
CKE0_B	E21	DIO	DRAM interface	DDRV
DMI0_B	B24	DIO	DRAM interface	DDRV
CA5_B	C22	DIO	DRAM interface	DDRV
DQ3_B	A24	DIO	DRAM interface	DDRV
DQ2_B	C23	DIO	DRAM interface	DDRV
DQ5_B	B25	DIO	DRAM interface	DDRV

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Pin name	Pin #	Type	Description	Power domain
DQ6_B	B26	DIO	DRAM interface	DDRV
DQS0_T_B	C25	DIO	DRAM interface	DDRV
DQS0_C_B	D25	DIO	DRAM interface	DDRV
DQ0_B	D24	DIO	DRAM interface	DDRV
DQ1_B	E23	DIO	DRAM interface	DDRV
DQ7_B	C26	DIO	DRAM interface	DDRV
DQ4_B	A26	DIO	DRAM interface	DDRV
EXTDN	B4	DIO	DRAM interface	DDRV
RESETN	E25	DIO	DRAM interface	DDRV
CAM				
CAM_CLK0	AA5	DIO	Master clock to 1st sensor	DVDD18_IORB
CAM_CLK1	AB5	DIO	Master clock to 2nd sensor	DVDD18_IORB
CAM_RST0	AB1	DIO	Reset control to 1st sensor	DVDD18_IORB
CAM_PDN0	AA2	DIO	Power down to 1st sensor	DVDD18_IORB
CAM_RST1	AA1	DIO	Reset control to 2nd sensor	DVDD18_IORB
CAM_PDN1	Y2	DIO	Power down to 2nd sensor	DVDD18_IORB
I2C				
SCL0	AF3	DIO	I2C0 clock	DVDD18_IORB
SCL1	AG3	DIO	I2C1 clock	DVDD18_IORB
SCL2	W1	DIO	I2C2 clock	DVDD18_IORB
SCL3	AJ31	DIO	I2C3 clock	DVDD18_IOLB
SCL4	W5	DIO	I2C3 clock	DVDD18_IORB
SCL_APPM	AL31	DIO	I2C3 clock	DVDD18_IOLB
SDA0	AH3	DIO	I2C0 data	DVDD18_IORB
SDA1	AH4	DIO	I2C1 data	DVDD18_IORB
SDA2	W2	DIO	I2C2 data	DVDD18_IORB
SDA3	AH29	DIO	I2C2 data	DVDD18_IOLB
SDA4	W4	DIO	I2C2 data	DVDD18_IORB
SDA_APPM	AK31	DIO	I2C3 data	DVDD18_IOLB
CONN				
WB_CTRL0	B2	DIO	WB control for CONN_RF	DVDD18_IORT2
WB_CTRL1	E4	DIO	WB control for CONN_RF	DVDD18_IORT2
WB_CTRL2	D4	DIO	WB control for CONN_RF	DVDD18_IORT2
WB_CTRL3	C3	DIO	WB control for CONN_RF	DVDD18_IORT2
WB_CTRL4	B3	DIO	WB control for CONN_RF	DVDD18_IORT2
WB_CTRL5	E5	DIO	WB control for CONN_RF	DVDD18_IORT2
WB_RSTB	M5	DIO	Reset for CONN_RF	DVDD18_IORT
WB_SEN	K4	DIO	SPI for CONN_RF	DVDD18_IORT
WB_SCLK	L4	DIO	SPI for CONN_RF	DVDD18_IORT
WB_SDATA	L6	DIO	SPI for CONN_RF	DVDD18_IORT
F2W_CLK	K5	DIO	AUD_IN from CONN_RF	DVDD18_IORT
F2W_DATA	K6	DIO	AUD_IN from CONN_RF	DVDD18_IORT

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Pin name	Pin #	Type	Description	Power domain
ABB				
DRX_BB2_QP	AJ15	AIO	DRX_BB2_QP	AVDD18_MD
DRX_BB2_QN	AK15	AIO	DRX_BB2_QN	AVDD18_MD
DRX_BB2_IN	AK16	AIO	DRX_BB2_IN	AVDD18_MD
DRX_BB2_IP	AK17	AIO	DRX_BB2_IP	AVDD18_MD
PRX_BB2_QP	AM14	AIO	PRX_BB2_QP	AVDD18_MD
PRX_BB2_QN	AM15	AIO	PRX_BB2_QN	AVDD18_MD
PRX_BB2_IN	AN15	AIO	PRX_BB2_IN	AVDD18_MD
PRX_BB2_IP	AN16	AIO	PRX_BB2_IP	AVDD18_MD
TX_BBQP	AM10	AIO	TX_BBQP	AVDD18_MD
TX_BBQN	AM11	AIO	TX_BBQN	AVDD18_MD
TX_BBIN	AN10	AIO	TX_BBIN	AVDD18_MD
TX_BBIP	AN9	AIO	TX_BBIP	AVDD18_MD
PRX_BB1_QP	AJ8	AIO	PRX_BB1_QP	AVDD18_MD
PRX_BB1_QN	AK8	AIO	PRX_BB1_QN	AVDD18_MD
PRX_BB1_IN	AK7	AIO	PRX_BB1_IN	AVDD18_MD
PRX_BB1_IP	AJ7	AIO	PRX_BB1_IP	AVDD18_MD
DRX_BB1_QP	AN7	AIO	DRX_BB1_QP	AVDD18_MD
DRX_BB1_QN	AN6	AIO	DRX_BB1_QN	AVDD18_MD
DRX_BB1_IN	AM6	AIO	DRX_BB1_IN	AVDD18_MD
DRX_BB1_IP	AM5	AIO	DRX_BB1_IP	AVDD18_MD
APC1	AL6	AIO	Automatic power control for modem	AVDD18_MD
MAIN_X26M_IN	AH16	AIO	26MHz clock input for AP and modem	AVDD18_MD
DET_BBIN	AL13	AIO	DET_BBIN	AVDD18_MD
DET_BBIP	AK13	AIO	DET_BBIP	AVDD18_MD
DET_BBQP	AN13	AIO	DET_BBQP	AVDD18_MD
DET_BBQN	AN12	AIO	DET_BBQN	AVDD18_MD
AUXIN0	AL19	AIO	AuxADC external input channel 0	AVDD18_MD
AUXIN1	AL18	AIO	AuxADC external input channel 1	AVDD18_MD
AUXIN2	AN18	AIO	AuxADC external input channel 2	AVDD18_MD
AUXIN3	AM18	AIO	AuxADC external input channel 3	AVDD18_MD
AUXIN4	AM17	AIO	AuxADC external input channel 4	AVDD18_MD
REFP	AN19	AIO	REFP	AVDD18_MD
REFN	AM19	AIO	REFN	AVDD18_MD
RFIC_ET_N	AK11	AIO	Envelope tracking	AVDD18_MD
RFIC_ET_P	AK10	AIO	Envelope tracking	AVDD18_MD
MIPI				
TDN0	K30	AIO	DSI0 lane 0 N	AVDD18_MIPITX
TDN0_A	N31	AIO	DSI0 lane 0 N	AVDD18_MIPITX
TDP0	K31	AIO	DSI lane 0 P	AVDD18_MIPITX
TDP0_A	N32	AIO	DSI lane 0 P	AVDD18_MIPITX
TDN1	L29	AIO	DSI lane 1 N	AVDD18_MIPITX

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Pin name	Pin #	Type	Description	Power domain
TDN1_A	R31	AIO	DSI lane 1 N	AVDD18_MIPITX
TDP1	K29	AIO	DSI0 lane 1 P	AVDD18_MIPITX
TDP1_A	P31	AIO	DSI0 lane 1 P	AVDD18_MIPITX
TDN2	M28	AIO	DSI0 lane 2 N	AVDD18_MIPITX
TDN2_A	P29	AIO	DSI0 lane 2 N	AVDD18_MIPITX
TDP2	N27	AIO	DSI0 lane 2 P	AVDD18_MIPITX
TDP2_A	P30	AIO	DSI0 lane 2 P	AVDD18_MIPITX
TDN3	M30	AIO	DSI0 lane 3 N	AVDD18_MIPITX
TDN3_A	T28	AIO	DSI0 lane 3 N	AVDD18_MIPITX
TDP3	M29	AIO	DSI0 lane 3 P	AVDD18_MIPITX
TDP3_A	R28	AIO	DSI0 lane 3 P	AVDD18_MIPITX
TCN	M31	AIO	DSI0 CK lane N	AVDD18_MIPITX
TCN_A	P28	AIO	DSI0 CK lane N	AVDD18_MIPITX
TCP	L31	AIO	DSI0 CK lane P	AVDD18_MIPITX
TCP_A	R27	AIO	DSI0 CK lane P	AVDD18_MIPITX
VRT	J30	AO	External resistor for DSI bias Connect 1.5K ohm 1% resistor to ground.	AVDD18_MIPITX
VRT_A	M32	AO	External resistor for DSI bias Connect 1.5K ohm 1% resistor to ground.	AVDD18_MIPITX
RDN0	W3	AIO	CSI0 lane0 N	AVDD18_MIPIRX0
RDP0	V3	AIO	CSI0 lane0 P	AVDD18_MIPIRX0
RDN1	V2	AIO	CSI0 lane1 N	AVDD18_MIPIRX0
RDP1	V1	AIO	CSI0 lane 1 P	AVDD18_MIPIRX0
RDN2	U2	AIO	CSI0 lane2 N	AVDD18_MIPIRX0
RDP2	U3	AIO	CSI0 lane2 P	AVDD18_MIPIRX0
RDN3	T2	AIO	CSI0 lane3 N	AVDD18_MIPIRX0
RDP3	T1	AIO	CSI0 lane3 P	AVDD18_MIPIRX0
RCN	U5	AIO	CSI0 CK lane N	AVDD18_MIPIRX0
RCP	U4	AIO	CSI0 CK lane P	AVDD18_MIPIRX0
RDN0_A	R3	AIO	CSI1 lane 0 N	AVDD18_MIPIRX1
RDP0_A	T3	AIO	CSI1 lane 0 P	AVDD18_MIPIRX1
RDN1_A	T5	AIO	CSI1 lane 1 N	AVDD18_MIPIRX1
RDP1_A	R5	AIO	CSI1 lane 1 P	AVDD18_MIPIRX1
RDN2_A	P2	AIO	CSI1 lane 2 N	AVDD18_MIPIRX1
RDP2_A	R2	AIO	CSI1 lane 2 P	AVDD18_MIPIRX1
RDN3_A	P1	AIO	CSI1 lane 3 N	AVDD18_MIPIRX1
RDP3_A	R1	AIO	CSI1 lane 3 P	AVDD18_MIPIRX1
RCN_A	N3	AIO	CSI1 CK lane N	AVDD18_MIPIRX1
RCP_A	P3	AIO	CSI1 CK lane P	AVDD18_MIPIRX1
USB				
USB_DM_P0	D31	AIO	USB D+ differential data line	AVDD33_USB_P0

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Pin name	Pin #	Type	Description	Power domain
USB_DP_P0	D32	AIO	USB D- differential data line	AVDD33_USB_P0
USB_DM_P1	H27	AIO	USB D+ differential data line	AVDD33_USB_P1
USB_DP_P1	H28	AIO	USB D- differential data line	AVDD33_USB_P1
CHD_DM_P0	E29	AIO	BC1.1 charger DP	AVDD33_USB_P0
CHD_DP_P0	E30	AIO	BC1.1 charger DM	AVDD33_USB_P0
SSUSB_XTALI	#N/A	AIO	SSUSB_XTALI	AVDD18_SSUSB
SSUSB_VRT	F31	AIO	SSUSB_VRT	AVDD18_SSUSB
SSUSB_TXP	G30	AIO	SSUSB_TXP	AVDD18_SSUSB
SSUSB_TXN	G29	AIO	SSUSB_TXN	AVDD18_SSUSB
SSUSB_RXP	H32	AIO	SSUSB_RXP	AVDD18_SSUSB
SSUSB_RXN	H31	AIO	SSUSB_RXN	AVDD18_SSUSB
WBG				
WB_RXQN	E2	AIO	RX_QN for WIFI/BT Rx	AVDD18_WBG
WB_RXQP	D2	AIO	RX_QP for WIFI/BT Rx	AVDD18_WBG
WB_RXIP	C1	AIO	RX_IN for WIFI/BT Rx	AVDD18_WBG
WB_RXIN	D1	AIO	RX_IP for WIFI/BT Rx	AVDD18_WBG
WB_TXQP	G3	AIO	TX_QP for WIFI/BT Tx	AVDD18_WBG
WB_TXQN	H3	AIO	TX_QN for WIFI/BT Tx	AVDD18_WBG
WB_TXIN	F1	AIO	TX_IN for WIFI/BT Tx	AVDD18_WBG
WB_TXIP	F2	AIO	TX_IP for WIFI/BT Tx	AVDD18_WBG
GPS_RXQN	K2	AIO	RX_QN for GPS Rx	AVDD18_WBG
GPS_RXQP	J2	AIO	RX_QP for GPS Rx	AVDD18_WBG
GPS_RXIP	H1	AIO	RX_IN for GPS Rx	AVDD18_WBG
GPS_RXIN	J1	AIO	RX_IP for GPS Rx	AVDD18_WBG
XIN_WBG	J4	AIO	26MHz clock input for WBG	AVDD18_WBG
MISC				
DRVBUS	AG32	DIO	USB OTG	
IDDIG	AF28	DIO	USB OTG	
TN_PLLGP	AB19	AIO	Reserved	
TP_PLLGP	AC19	AIO	Reserved	
TN_MEMPLL	C18	AIO	Reserved	
TP_MEMPLL	D18	AIO	Reserved	
Analog Power				
AVDD18_AP	AM20	P	Analog power input 1.8V	
AVDD18_MD	AL20	P	Analog power input 1.8V for modem	
AVDD18_MDPLLGP	W19	P	Analog power input 1.8V for PLL	
AVDD18_MIPIRX0	N2	P	Analog power for MIPI CSI	
AVDD18_MIPIRX1	N1	P	Analog power for MIPI CSI	
AVDD18_MIPITX	K32	P	Analog power for MIPI	
AVDD18_USB	E31	P	Analog power 1.8V for USB	

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Pin name	Pin #	Type	Description	Power domain
AVDD18_WBG	L1	P	Analog power 1.8V for WBG	
AVDD28_DAC	AN4	P	Analog power 1.8V for DAC	
AVDD18_SSUSB	F32	P	Analog power 1.8V for SSUSB	
AVDD10_SSUSB	G31	P	Analog power 1.0V for SSUSB	
AVDD18_USB	E31	P	Analog power 1.8V for USB	
AVDD33_USB_P0	C32	P	Analog power 3.3V for USB	
AVDD33_USB_P1	C31	P	Analog power 3.3V for USB	
Digital Power				
VDD2	F11	P	Digital power input for DDR	-
VDDQ	F13	P	Digital power input for DDR	-
DVDD_CORE	K8	P	Digital power input for DDR	-
DVDD_PROC	V20	P	Digital power input for DVFS	-
DVDD_GPU	G25	P	Digital power input for GPU	-
DVDD_MODEM	U8	P	Digital power input for LTE	-
DVDD_SRAM_CORE	K12	P	Digital power input for LTE	-
DVDD_MD1	P11	P	Digital power input for LTE	-
DVDD_SRAM	AB20	P	Digital power input for SRAM	-
DVDD_CORE	K8	P	Digital power input for TOP	-
DVDD18_IOLT	R32	P	Digital power input for IO	-
DVDD18_IOLB	AL32	P	Digital power input for IO	
DVDD18_IOLB	AN21	P	Digital power input for IO	
DVDD18_IORB	AF1	P	Digital power input for IO	-
DVDD18_IORB	AJ1	P	Digital power input for IO	
DVDD18_IORT1	M1	P	Digital power input for IO	
DVDD18_IORT2	A3	P	Digital power input for IO	
DVDD18_MSDC0	A30	P	Digital power input for MSDC0	
DVDD18_MC1	AB32	P	Digital power input for MSDC1	
DVDD28_MSDC1	AB31	P	Digital power input for MSDC1	
DVDD18_SIM	AE32	P	Digital power input for SIM1/2	
DVDD28_SIM1	AF31	P	Digital power input for SIM1	
DVDD28_SIM2	AE31	P	Digital power input for SIM2	
Analog Ground				
AVSS18_MD	AF10	G	Analog ground input for modem	
AVSS18_MDPLLGP	Y19	G	Analog ground input for PLL	
AVSS18_MIPIRX	P6	G	Analog ground input for MIPI RX	
AVSS18_MIPITX	N26	G	Analog ground input for MIPI TX	
AVSS18_WBG	C2	G	Analog ground input for WBG	
AVSS33_USB	F29	G	Analog ground input for USB	
AVSS10_SSUSB	H30	G	Analog ground input for SSUSB	

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Pin name	Pin #	Type	Description	Power domain
Digital Ground				
GND		G		-

Table 2-4. Acronym for table of state of pins

Abbreviation	Description
I	Input
LO	Low output
HO	High output
XO	Low or high output
PU	Pull-up
PD	Pull-dowm
-	No PU/PD
0~N	Aux. function number
X	Delicate function pin

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2.2 Electrical Characteristic

2.2.1 Absolute Maximum Ratings

Table 2-5. Absolute maximum ratings for power supply

Symbol or pin name	Description	Max.	Unit
AVDD18_DDR AVDD18_MDPLLGP	Analog power input 1.8V for PLL & DDR	1.89	V
AVDD18_AP	Analog power input 1.8V for AuxADC, TSENSE	1.89	V
AVDD18_MD	Analog power input 1.8V for BBTX, BBRX	1.89	V
AVDD28_DAC	Analog power input 2.8V for APC	2.94	V
AVDD18_MIPITX	Analog power for MIPI DSI	1.89	V
AVDD18_MIPIRX0 AVDD18_MIPIRX1	Analog power for MIPI CSI0 & CSI1	1.89	V
AVDD33_USB_P0 AVDD33_USB_P1	Analog power 3.3V for USB	3.22	V
AVDD18_USB	Analog power 1.8V for USB	1.89	V
AVDD18_SSUSB	Analog power 1.8V for SSUSB	1.89	V
AVDD10_SSUSB	Analog power 1.0V for SSUSB	1.05	V
AVDD18_WBG	Analog power 1.8V for connectivity ABB	1.89	V
DVDD18_IOLT DVDD18_SIM DVDD18_IOLB DVDD18_IOBL DVDD18_IOBR DVDD18_IORB DVDD18_IORT1 DVDD18_IORT2 DVDD18_BIAS1 DVDD18_BIAS2 DVDD18_BIAS3 DVDD18_MC1	Digital power input for 1.8V IO	1.98	V
DVDD18_MSDC0	Digital power input for MSDC0	1. 95	V
DVDD28_MSDC1	Digital power input for MSDC1	3.3	V
DVDD28_SIM1	Digital power input for SIM1	3.3	V
DVDD28_SIM2	Digital power input for SIM2	3.3	V
DDRV DDRV_CLK DDRV_VREF	Digital power input for DRAM	1.155	V
DVDD_PROC	Digital power input for DVFS	1.076	V
DVDD_GPU	Digital power input for GPU	0.945	V
DVDD_MD1	Digital power input for MD1	0.735	V
DVDD_SRAM_MODEM	Digital power input for MD SRAM	1.05	V
DVDD_MODEM	Digital power input for MODEM	0.84	V
DVDD_SRAM	Digital power input for SRAM	0.945	V
DVDD_CORE	Digital power input for TOP	0.84	V

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Warning: *Stressing the device beyond the absolute maximum ratings may cause permanent damage. These are stress ratings only.*

2.2.2 Recommended Operating Conditions

Table 2-6. Recommended operating conditions for power supply

Symbol or pin name	Description	Min.	Typ.	Max.	Unit
AVDD18_DDR AVDD18_MDPLLGP	Analog power input 1.8V for PLL & DDR	1.71	1.8	1.89	V
AVDD18_AP	Analog power input 1.8V for AuxADC, TSENSE	1.71	1.8	1.89	V
AVDD18_MD	Analog power input 1.8V for BBTX, BBRX	1.71	1.8	1.89	V
AVDD28_DAC	Analog power input 2.8V for APC	2.66	2.8	2.94	V
AVDD18_MIPITX	Analog power for MIPI DSI	1.71	1.8	1.89	V
AVDD18_MIPIRX0 AVDD18_MIPIRX1	Analog power for MIPI CSI0 & CSI1	1.71	1.8	1.89	V
AVDD33_USB_P0 AVDD33_USB_P1	Analog power 3.3V for USB	2.92	3.07	3.22	V
AVDD18_USB	Analog power 1.8V for USB	1.71	1.8	1.89	V
AVDD18_SSUSB	Analog power 1.8V for SSUSB	1.71	1.8	1.89	V
AVDD10_SSUSB	Analog power 1.0V for SSUSB	0.95	1	1.05	V
AVDD18_WBG	Analog power 1.8V for connectivity ABB	1.71	1.8	1.89	V
DVDD18_IOLT DVDD18_SIM DVDD18_IOLB DVDD18_IOBL DVDD18_IOBR DVDD18_IORB DVDD18_IORT1 DVDD18_IORT2 DVDD18_BIAS1 DVDD18_BIAS2 DVDD18_BIAS3 DVDD18_MC1	Digital power input for 1.8V IO	1.62	1.8	1.98	V
DVDD18_MSDC0	Digital power input for MSDC0	1.7	1.8	1.95	V
DVDD28_MSDC1	Digital power input for MSDC1	1.7 2.7	1.8 3.0	1.9 3.3	V
DVDD28_SIM1 DVDD28_SIM2	Digital power input for SIM1/SIM2	2.7 1.68	3 1.8	3.3 1.92	V
DDRV DDRV_CLK DDRV_VREF	Digital power input for EMI (LPDDR3/4)	1.045	1.1	1.155	V
DVDD_PROC	Digital power input for DVFS	0.57 0.665 0.76 0.855	0.6 0.7 0.8 0.9	0.63 0.735 0.84 0.945	V

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Symbol or pin name	Description	Min.	Typ.	Max.	Unit
		0.973	1.025	1.076	
DVDD_GPU	Digital power input for GPU	0.855	0.9	0.945	V
		0.76	0.8	0.84	
		0.665	0.7	0.735	
		0.617	0.65	0.682	
		0.57	0.6	0.63	
DVDD_MD1	Digital power input for MD1	0.665	0.7	0.735	V
DVDD_SRAM_MODEM	Digital power input for MD SRAM	0.95	1.0	1.05	V
		0.855	0.9	0.945	V
DVDD_MODEM	Digital power input for MODEM	0.76	0.8	0.84	V
		0.665	0.7	0.735	
DVDD_SRAM	Digital power input for SRAM	0.855	0.9	0.945	V
DVDD_CORE	Digital power input for TOP	0.76	0.8	0.84	V
		0.665	0.7	0.735	

2.2.3 Storage Condition

1. Shelf life in sealed bag: 12 months at < 40°C and < 90% relative humidity (RH).
2. After the bag is opened, devices subject to infrared reflow, vapor-phase reflow or equivalent processing must be:
   - Mounted within 168 hours in factory condition of 30°C/60% RH, or
   - Stored at 20% RH
3. Devices require baking before being mounted, if they are placed
   - For 192 hours at 40°C +5°C/-0°C and < 5% RH in low temperature device containers, or
   - For 24 hours at 125°C +5°C/-0°C in high temperature device containers.

2.2.4 DC Electrical Characteristics

2.2.4.1 RTC DC Electrical Characteristics

Table 2-7. RTC DC electrical characteristics (DVDD18_IOLT =1.8V)

Parameters	Descriptions	Min.	Typ.	Max.	Unit
VIH	Input logic low voltage	0.65*DVDD18_IOLT		DVDD18_IOLT + 0.3	V
VIL	Input logic high voltage	-0.3		0.35*DVDD18_IOLT	V
VOH	DC output logic low voltage	0.75*DVDD18_IOLT			V
VOL	DC output logic high voltage			0.25*DVDD18_IOLT	V
FRTC	Input clock frequency		32		kHz
DCRTC	Input signal duty cycle	45	50	55	%

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2.2.4.2 SPI, I2S DC Electrical Characteristics

Table 2-8. SPI, I2S DC electrical characteristics (DVDD18_IORB =1.8V)

Parameters	Descriptions	Min.	Typ.	Max.	Unit
VIH	Input logic low voltage	0.65*DVDD18_IORB		DVDD18_IORB + 0.3	V
VIL	Input logic high voltage	-0.3		0.35*DVDD18_IORB	V
VOH	DC output logic low voltage	0.75*DVDD18_IORB			V
VOL	DC Output logic high voltage			0.25*DVDD18_IORB	V

2.2.4.3 I2C0, I2C1, I2C2 DC Electrical Characteristics

Table 2-9. I2C0, I2C1, I2C2 DC electrical characteristics (DVDD18_IORB =1.8V)

Parameters	Descriptions	Min.	Typ.	Max.	Unit
VIH	Input logic low voltage	0.65*DVDD18_IORB		DVDD18_IORB + 0.3	V
VIL	Input logic high voltage	-0.3		0.35*DVDD18_IORB	V
VOL	DC output logic high voltage			0.2*DVDD18_IORB	V

2.2.4.4 I2C3 DC Electrical Characteristics

Table 2-10. I2C3 DC electrical characteristics (DVDD18_IOLB =1.8V)

Parameters	Descriptions	Min.	Typ	Max.	Unit
VIH	Input logic low voltage	0.65*DVDD18_IOLB		DVDD18_IOLB + 0.3	V
VIL	Input logic high voltage	-0.3		0.35*DVDD18_IOLB	V
VOL	DC output logic high voltage			0.2*DVDD18_IOLB	V

2.2.4.5 MSDC0 DC Electrical Characteristics

Table 2-11. MSDC0 DC electrical characteristics (DVDD28_MSDC0=1.8V)

Parameters	Descriptions	Min.	Typ.	Max.	Unit
VIH	Input logic low voltage	1.3		2.0	V
VIL	Input logic high voltage	-0.3		0.58	V
VOH	DC output logic low voltage	1.4			V
VOL	DC output logic high voltage			0.45	V

2.2.4.6 MSDC1 DC Electrical Characteristics

Table 2-12. MSDC1 DC electrical characteristics (DVDD28_MSDC1=2.8V/3.3V)

Parameters	Descriptions	Min.	Typ.	Max.	Unit
VIH	Input logic low voltage	0.625*		DVDD28_MSDC1 + 0.3	V

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Parameters	Descriptions	Min.	Typ.	Max.	Unit
		DVDD28_MSDC1			
VIL	Input logic high voltage	-0.3		0.25* DVDD28_MSDC1	V
VOH	DC output logic low voltage	0.75* DVDD28_MSDC1		DVDD28_MSDC1 + 0.3	V
VOL	DC output logic high voltage	-0.3		0.125* DVDD28_MSDC1	V

Table 2-13. MSDC1 DC electrical characteristics (DVDD28_MSDC1=1.8V)

Parameters	Descriptions	Min	Typ	Max	Unit
VIH	Input logic low voltage	1.27		DVDD28_MSDC1 + 0.3	V
VIL	Input logic high voltage	-0.3		0.58	V
VOH	DC output logic low voltage	1.4		DVDD28_MSDC1 + 0.3	V
VOL	DC output logic high voltage	-0.3		0.45	V

2.2.4.7 SIM DC Electrical Characteristics

Table 2-14. SIM DC electrical characteristics

Parameter	Conditions	Symbol	Min.	Typ.	Max.	Unit
SIM1_SIO						
Input high voltage	DVDD28_SIM1 = 1.8V	V_{ih}	1.4	1.8	N/A	V
Input low voltage		V_{il}	N/A	0.0	0.27	V
Output high voltage		V_{oh}	1.4	1.8	1.9	V
Output low voltage		V_{ol}	N/A	0.0	0.27	V
Input high voltage	DVDD28_SIM1 = 3.0V	V_{ih}	2.6	3.0	N/A	V
Input low voltage		V_{il}	N/A	0.0	0.4	V
Output high voltage		V_{oh}	2.6	3.0	3.1	V
Output low voltage		V_{ol}	N/A	0.0	0.4	V
SIM1_SCLK						
Input high voltage	DVDD28_SIM1 = 1.8V	V_{ih}	1.4	1.8	N/A	V
Input low voltage		V_{il}	N/A	0.0	0.27	V
Output high voltage		V_{oh}	1.62	1.8	1.9	V
Output low voltage		V_{ol}	N/A	0.0	0.22	V
Input high voltage	DVDD28_SIM1 = 3.0V	V_{ih}	2.6	3.0	N/A	V
Input low voltage		V_{il}	N/A	0.0	0.4	V
Output high voltage		V_{oh}	2.7	3.0	3.1	V
Output low voltage		V_{ol}	N/A	0.0	0.4	V
SIM1_SRST						
Input high voltage	DVDD28_SIM1 = 1.8V	V_{ih}	1.4	1.8	N/A	V
Input low voltage		V_{il}	N/A	0.0	0.27	V
Output high voltage		V_{oh}	1.62	1.8	1.9	V

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Parameter	Conditions	Symbol	Min.	Typ.	Max.	Unit
Output low voltage		V_{ol}	N/A	0.0	0.36	V
Input high voltage	DVDD28_SIM1 = 3.0V	V_{ih}	2.6	3.0	N/A	V
Input low voltage		V_{il}	N/A	0.0	0.4	V
Output high voltage		V_{oh}	2.7	3.0	3.1	V
Output low voltage		V_{ol}	N/A	0.0	0.36	V
SIM2_SIO						
Input high voltage	DVDD28_SIM2 = 1.8V	V_{ih}	1.4	1.8	N/A	V
Input low voltage		V_{il}	N/A	0.0	0.27	V
Output high voltage		V_{oh}	1.4	1.8	1.9	V
Output low voltage		V_{ol}	N/A	0.0	0.27	V
Input high voltage	DVDD28_SIM2= 3.0V	V_{ih}	2.6	3.0	N/A	V
Input low voltage		V_{il}	N/A	0.0	0.4	V
Output high voltage		V_{oh}	2.6	3.0	3.1	V
Output low voltage		V_{ol}	N/A	0.0	0.4	V
SIM2_SCLK						
Input high voltage	DVDD28_SIM2 = 1.8V	V_{ih}	1.4	1.8	N/A	V
Input low voltage		V_{il}	N/A	0.0	0.27	V
Output high voltage		V_{oh}	1.62	1.8	1.9	V
Output low voltage		V_{ol}	N/A	0.0	0.22	V
Input high voltage	DVDD28_SIM2 = 3.0V	V_{ih}	2.6	3.0	N/A	V
Input low voltage		V_{il}	N/A	0.0	0.4	V
Output high voltage		V_{oh}	2.7	3.0	3.1	V
Output low voltage		V_{ol}	N/A	0.0	0.4	V
SIM2_SRST						
Input high voltage	DVDD28_SIM2 = 1.8V	V_{ih}	1.4	1.8	N/A	V
Input low voltage		V_{il}	N/A	0.0	0.27	V
Output high voltage		V_{oh}	1.62	1.8	1.9	V
Output low voltage		V_{ol}	N/A	0.0	0.36	V
Input high voltage	DVDD28_SIM2 = 3.0V	V_{ih}	2.6	3.0	N/A	V
Input low voltage		V_{il}	N/A	0.0	0.4	V
Output high voltage		V_{oh}	2.7	3.0	3.1	V
Output low voltage		V_{ol}	N/A	0.0	0.36	V

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2.2.5 AC Electrical Characteristics and Timing Diagram

2.2.5.1 External Memory Interface for LPDDR3

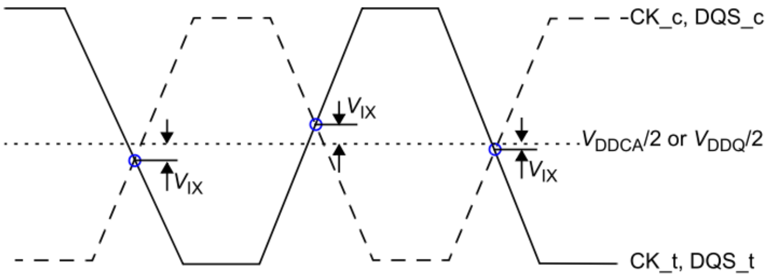

Figure 2-3. LPDDR3 VIX definition

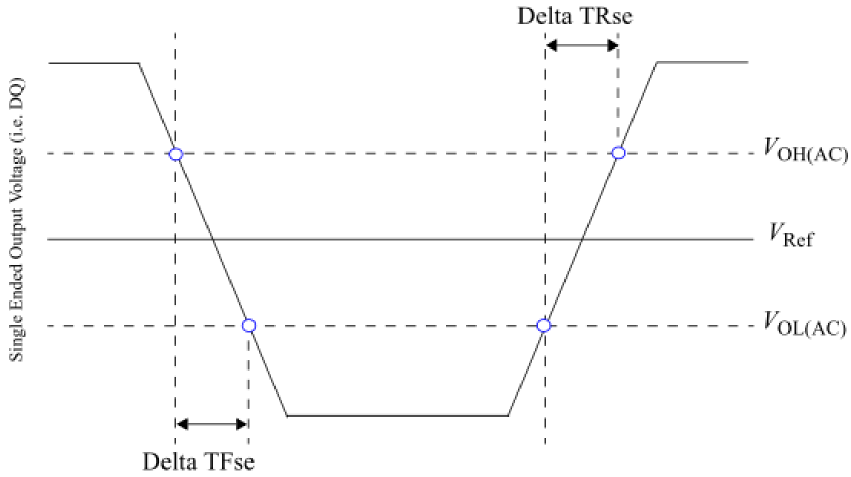

Figure 2-4. LPDDR3 single-ended output slew-rate definition

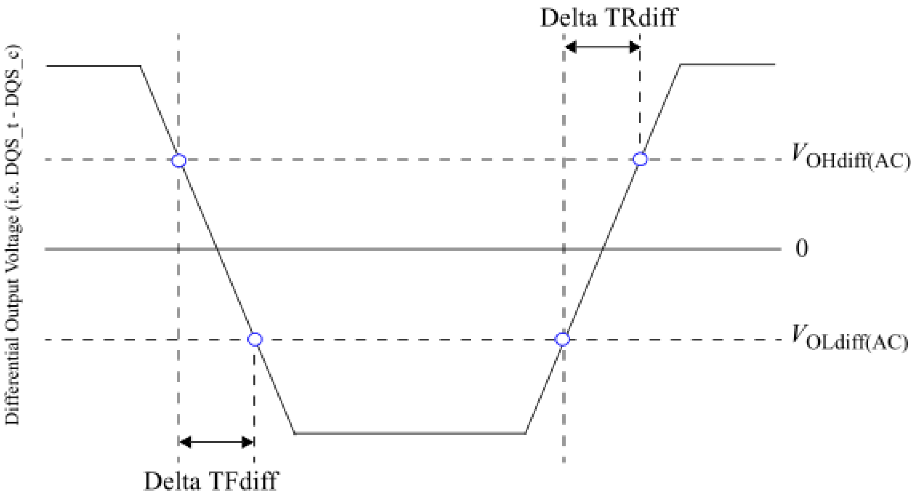

Figure 2-5. LPDDR3 differential output slew-rate definition

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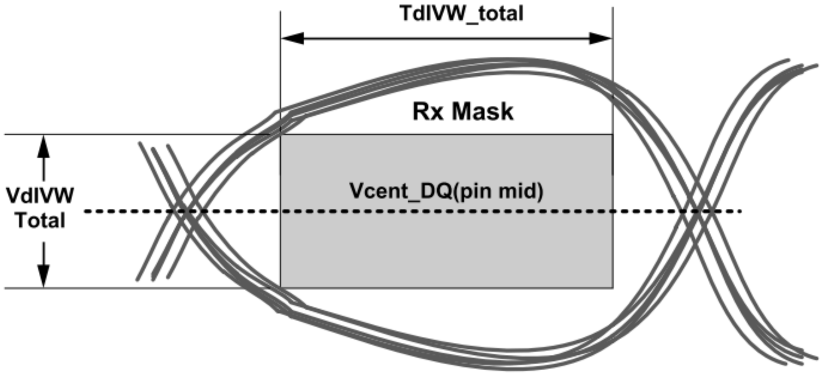

Figure 2-6. LPDDR3 RX mask

Table 2-15. LPDDR3 AC timing parameter table of external memory interface

Symbol	Description	Min.	Typ.	Max.	Unit
VIXCA	Differential Input Cross Point Voltage relative to VDDCA/2 for CK_t, CK_c	-120		120	mV
VIXDQ	Differential Input Cross Point Voltage relative to VDDQ/2 for DQS_t, DQS_c	-120		120	mV
SRQse	Single-ended Output Slew Rate (RON = 40Ω +/- 30%)	1.5		4	V/ns
SRQdiff	Differential Output Slew Rate (RON = 40Ω +/- 30%)	3		8	V/ns
VdIVW_total	Rx Mask voltage - p-p total			140	mV
TdIVW_total	Rx timing window total (At VdIVW voltage levels)			0.25	UI

2.2.5.2 External Memory Interface for LPDDR4/LPDDR4X

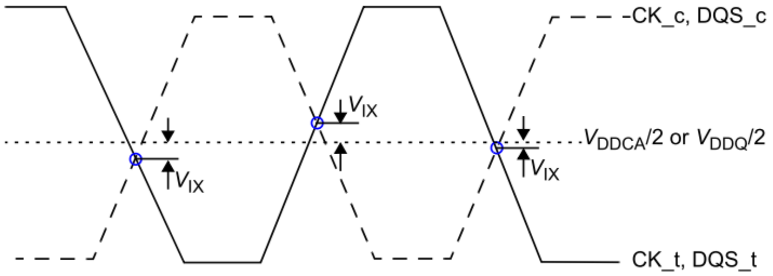

Figure 2-7. LPDDR4/LPDDR4X VIX definition

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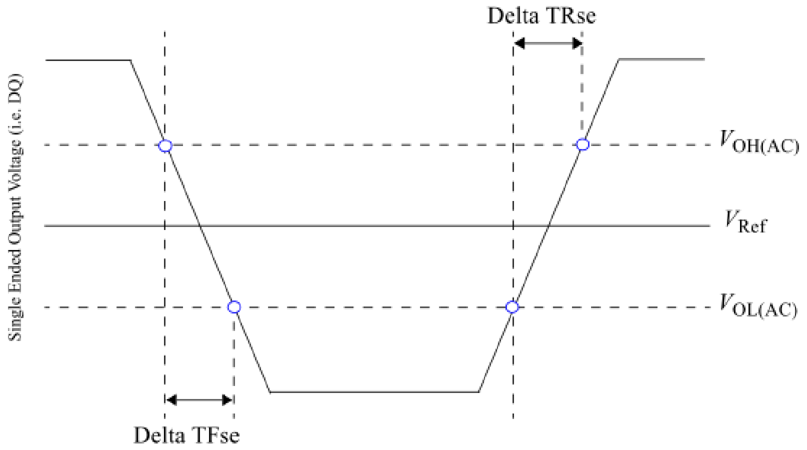

Figure 2-8. LPDDR4/LPDDR4X single-ended output slew-rate definition

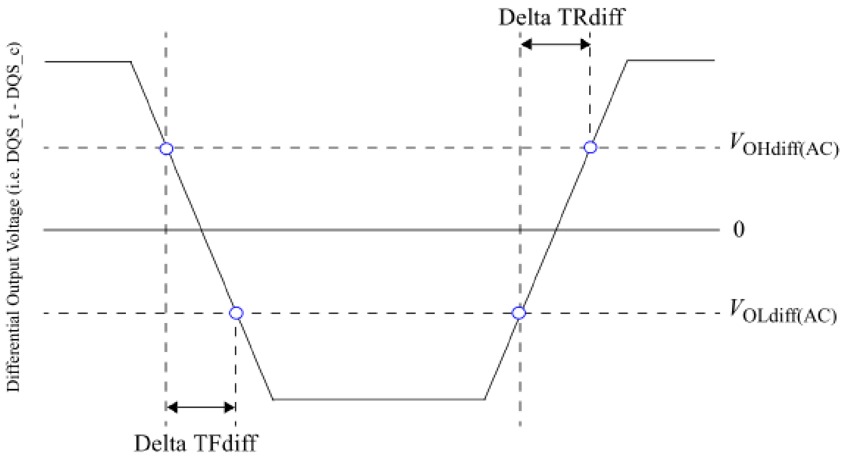

Figure 2-9. LPDDR4/LPDDR4X differential output slew-rate definition

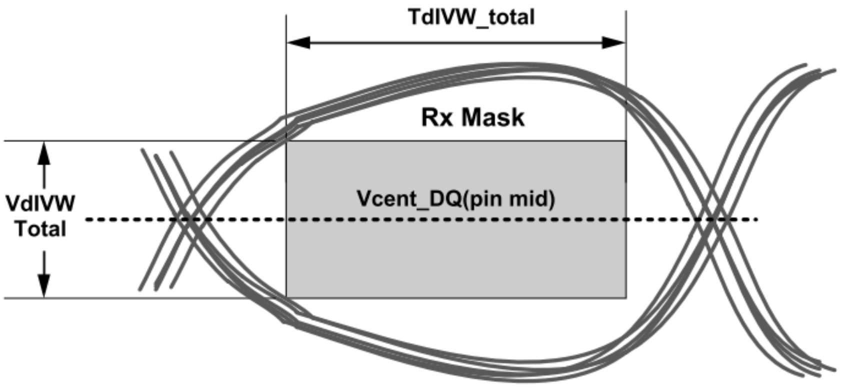

Figure 2-10. LPDDR4/LPDDR4X RX mask

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Table 2-16. LPDDR4/LPDDR4X AC timing parameter table of external memory interface

Symbol	Description	Min.	Typ.	Max.	Unit
Vix_DQS_ratio	DQS Differential input crosspoint voltage ratio			20	%
Vix_CK_ratio	CK Differential input crosspoint voltage ratio			25	%
SRQse (LPDDR4)	Single-ended Output Slew Rate	3.5		9	V/ns
SRQse (LPDDR4X)	Single-ended Output Slew Rate	3		9	V/ns
SRQdiff (LPDDR4)	Differential Output Slew Rate	7		18	V/ns
SRQdiff (LPDDR4X)	Differential Output Slew Rate	6		18	V/ns
VdIVW_total	Rx Mask voltage - p-p total			140	mV
TdIVW_total	Rx timing window total (At VdIVW voltage levels)			0.25	UI

2.2.5.3 SPI AC Timing Characteristics

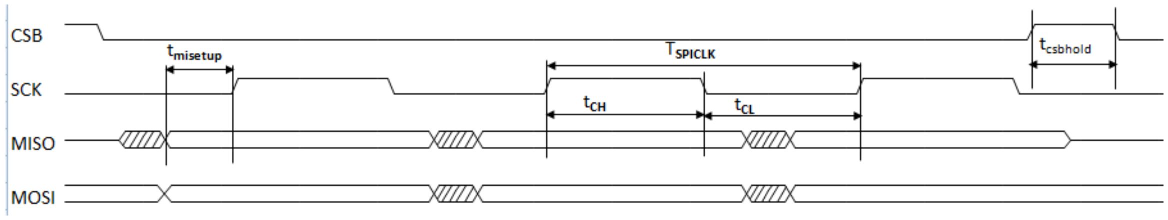

Figure 2-11. SPI timing diagram

Table 2-17. SPI AC timing parameters

Parameter	Symbol	Min.	Typ.	Max.	Unit
SPI clock period	T_{SPICLK}	18.2	-	-	ns
SPI clock low time	t_{CL}	9.1	-	-	ns
SPI clock high time	t_{CH}	9.1	-	-	ns
SPI CSB hold time	$t_{csbhold}$	9.1	-	-	ns
SPI MISO setup time (MISO 80%, SCK 20%)	$t_{misetup}$	28.5	-	-	ns

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2.2.5.4 I2S AC Timing Characteristics

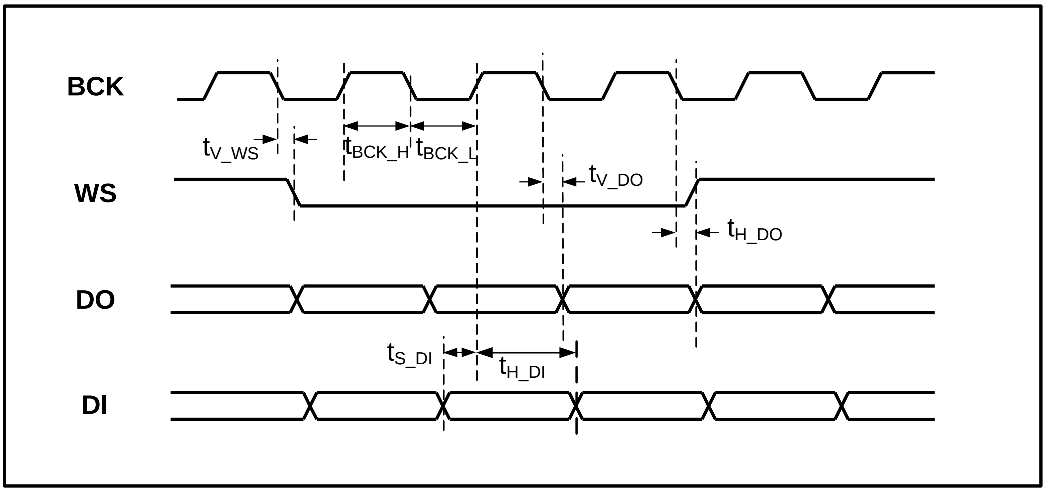

Figure 2-12. I2S master mode timing diagram

Table 2-18. I2S AC timing parameters

Parameter	Description	Min.	Typ.	Max.	Unit
f_S	Sampling frequency	8	-	192	kHz
t_{WS}	Word select period	32	-	64	$1/f_{BCK}$
f_{MCK}	Master clock frequency	-	-	24.576	MHz
f_{BCK}	Serial clock frequency	32 * f_S	-	64 * f_S	MHz
t_{BCK_H}	BCK high-level time	-	0.5	-	$1/f_{BCK}$
t_{BCK_L}	BCK low-level time	-	0.5	-	$1/f_{BCK}$
t_{V_WS}	WS valid time	-	-	0.2	$1/f_{BCK}$
t_{H_WS}	WS hold time	0	-	-	$1/f_{BCK}$
t_{V_DO}	DO valid time	-	-	0.2	$1/f_{BCK}$
t_{H_DO}	DO hold time	0	-	-	$1/f_{BCK}$
t_{S_DI}	DI setup time	0.2	-	-	$1/f_{BCK}$
t_{H_DI}	DI hold time	0.2	-	-	$1/f_{BCK}$

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2.2.5.5 I2C AC Timing Characteristics

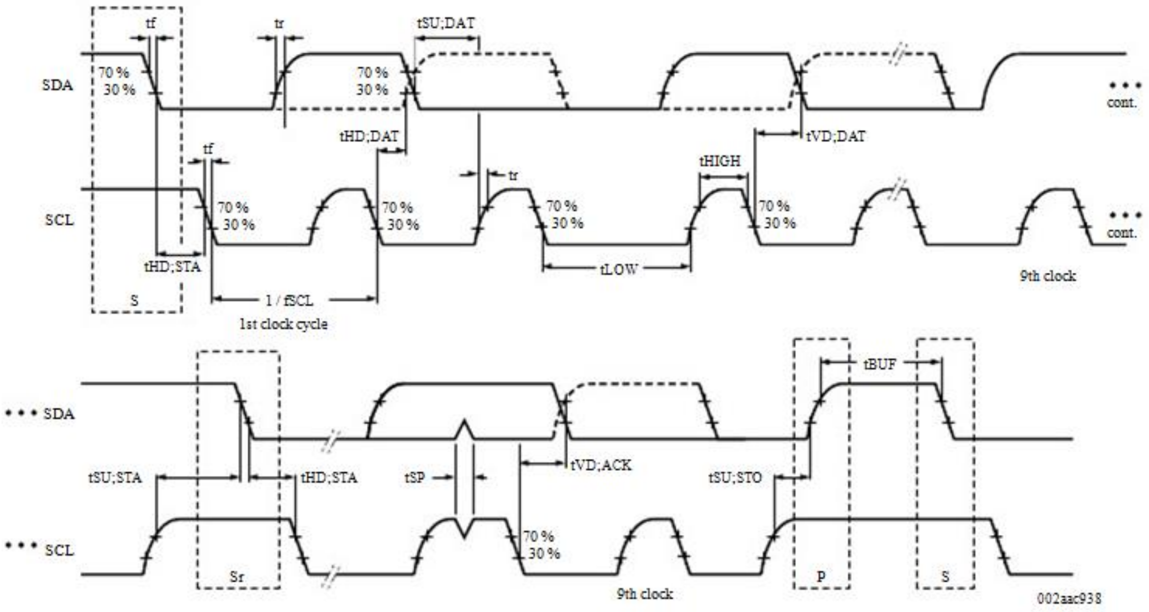

Figure 2-13. I2C timing diagram of standard mode (100kHz) and fast mode (400kHz)

Table 2-19. I2C AC timing parameters

Symbol	Standard mode	Fast mode	Unit	Note
$t_{HD;STA}$	2.5	0.625	µs	Can be extended by 0x28, extension configuration register.
t_{LOW}	5	1.25	µs	
t_{HIGH}	5	1.25	µs	
$t_{SU;STA}$	2.5	0.625	µs	
$t_{HD;DAT}$	2.5	0.625	µs	
$t_{SU;DAT}$	2.5	0.625	µs	
$t_{SU;STO}$	2.5	0.625	µs	Can be extended by 0x28, extension configuration register.

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2.2.5.6 MSDC AC Timing Characteristics

2.2.5.6.1 Default Speed Timing

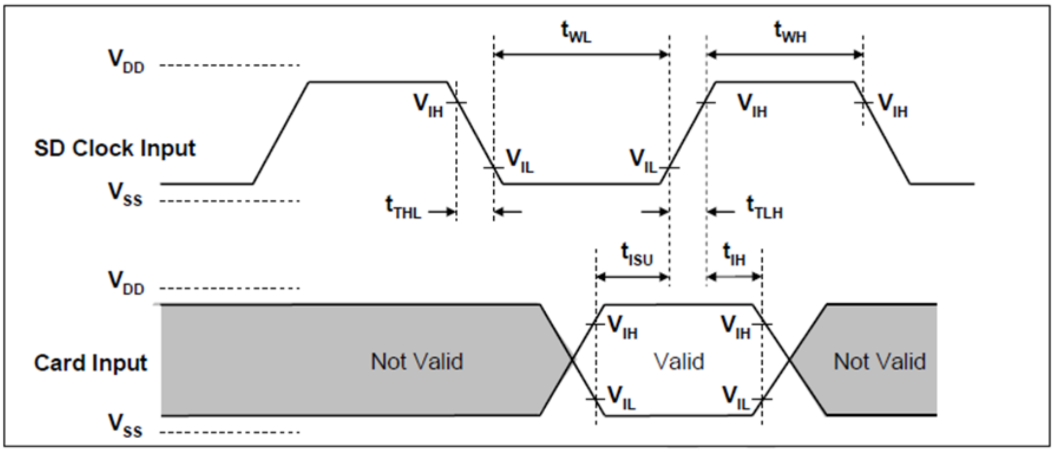

Figure 2-14. MSDC input timing diagram of default speed

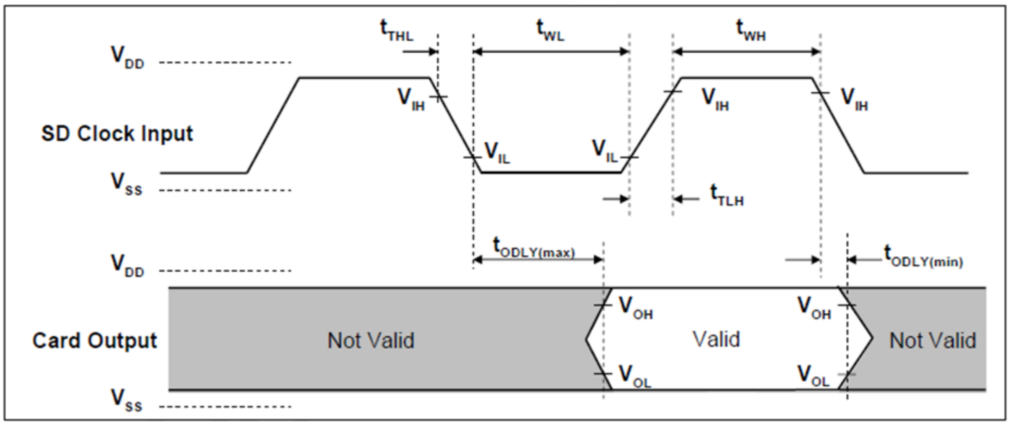

Figure 2-15. MSDC output timing diagram of default speed

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Table 2-20. MSDC AC timing parameters of default speed

Parameter	Symbol	Min.	Max.	Unit	Remark
Clock CLK (All values are referred to min (V_{IH}) and max (V_{IL}))					
Clock frequency data transfer mode	f_{PP}	0	25	MHz	C_{CARD}≦10pF (1 card)
Clock frequency identification mode	f_{OD}	0(1) / 100	400	kHz	C_{CARD}≦10pF (1 card)
Clock low time	t_{WL}	10		ns	C_{CARD}≦10pF (1 card)
Clock high time	t_{WH}	10		ns	C_{CARD}≦10pF (1 card)
Clock rise time	t_{TLH}		10	ns	C_{CARD}≦10pF (1 card)
Clock fall time	t_{THL}		10	ns	C_{CARD}≦10pF (1 card)
Input CMD, DAT (referenced to CLK)					
Input setup time	T_{ISU}	5		ns	C_{CARD}≦10pF (1 card)
Input hold time	T_{IH}	5		ns	C_{CARD}≦10pF (1 card)
Output CMD, DAT (referenced to CLK)					
Output delay time during data transfer mode	T_{ODLY}	0	14	ns	C_L≦40pF (1 card)
Output delay time during identification mode	T_{ODLY}	0	50	ns	C_L≦40pF (1 card)

2.2.5.6.2 High Speed Timing

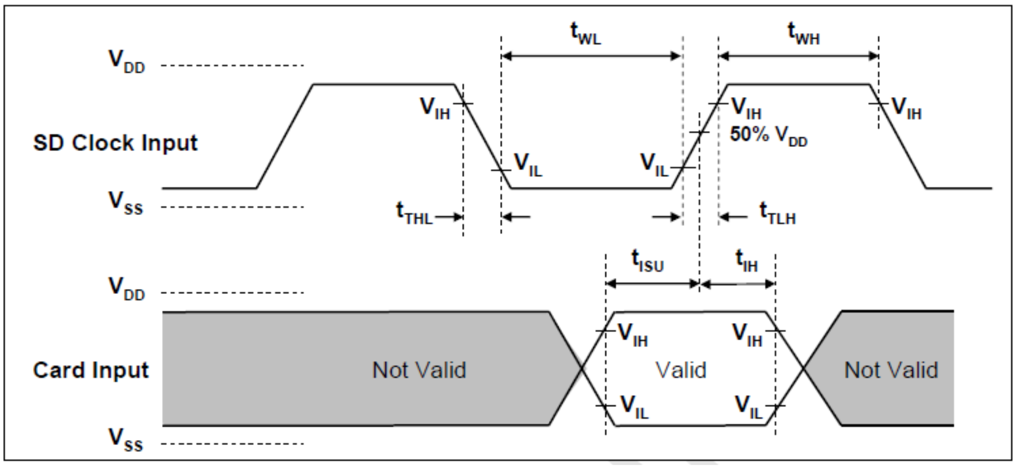

Figure 2-16. MSDC input timing diagram of high speed

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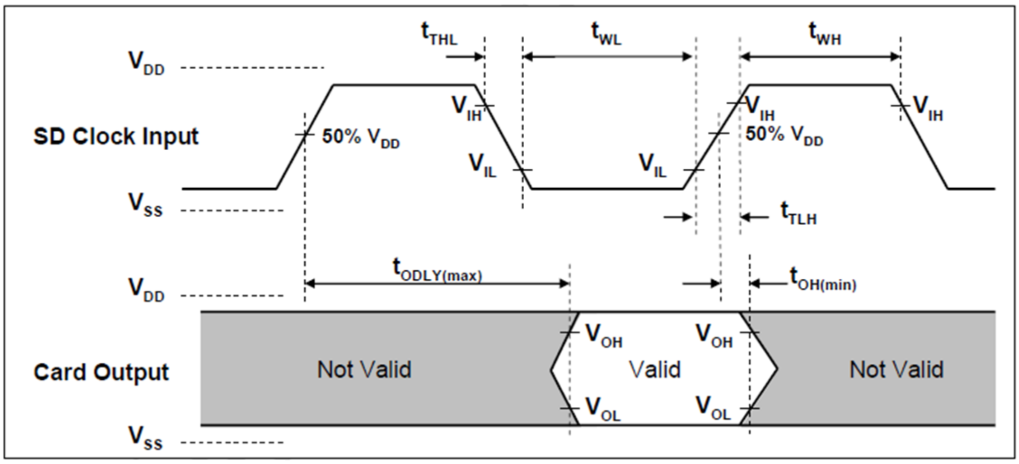

Figure 2-17. MSDC output timing diagram of high speed

Table 2-21. MSDC AC timing parameters of high speed

Parameter	Symbol	Min.	Max.	Unit	Remark
Clock CLK (All values are referred to min (V_{IH}) and max (V_{IL}))					
Clock frequency data transfer mode	f_{PP}	0	50	MHz	C_{CARD}≦10pF (1 card)
Clock low time	t_{WL}	7		ns	C_{CARD}≦10pF (1 card)
Clock high time	t_{WH}	7		ns	C_{CARD}≦10pF (1 card)
Clock rise time	t_{TLH}		3	ns	C_{CARD}≦10pF (1 card)
Clock fall time	t_{THL}		3	ns	C_{CARD}≦10pF (1 card)
Input CMD, DAT (referenced to CLK)					
Input setup time	t_{ISU}	6		ns	C_{CARD}≦10pF (1 card)
Input hold time	t_{IH}	2		ns	C_{CARD}≦10pF (1 card)
Output CMD, DAT (referenced to CLK)					
Output delay time during data transfer mode	t_{ODLY}		14	ns	C_L≦40pF (1 card)
Output hold time	t_{OH}	2.5		ns	C_L≧15pF (1 card)
Total system capacitance for each line	C_L		40	pF	1 card

2.2.5.6.3 SDR12/SDR25/SDR50/SDR104 Mode Timing

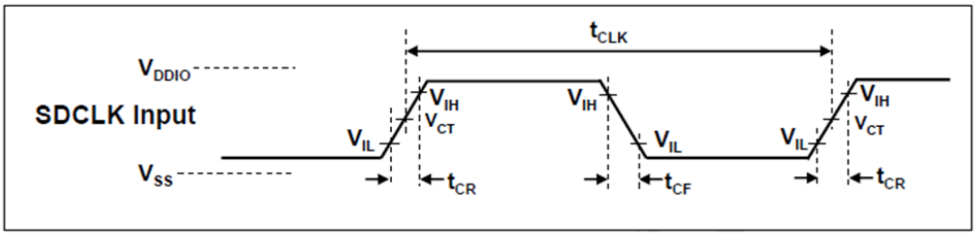

Figure 2-18. MSDC clock timing diagram of SDR12/SDR25/SDR50/SDR104 mode

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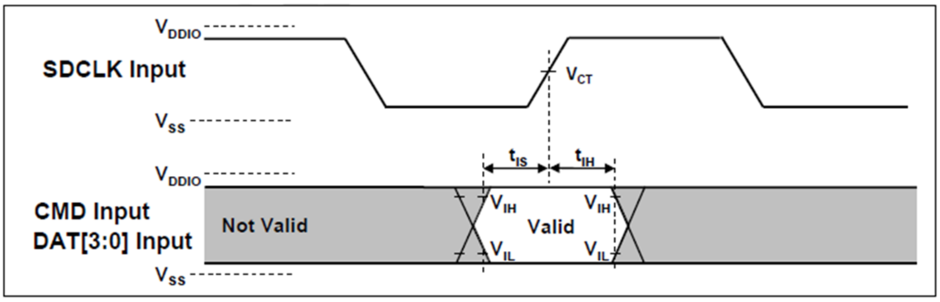

Figure 2-19. MSDC input timing diagram of SDR50/SDR104 mode

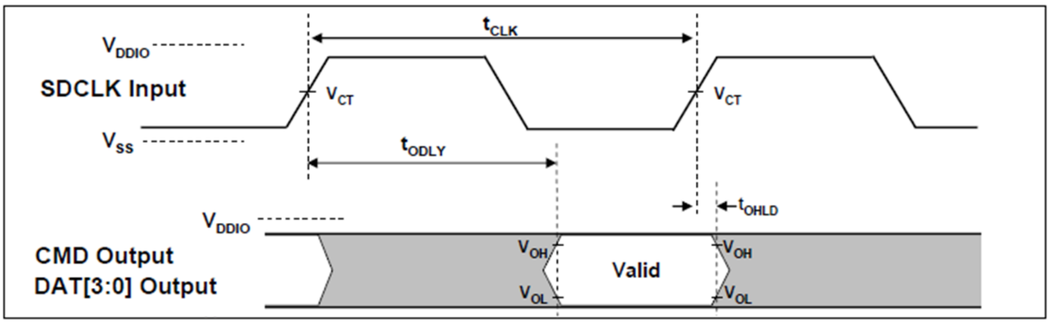

Figure 2-20. MSDC output timing diagram of fixed data window (SDR12/SDR25/SDR50)

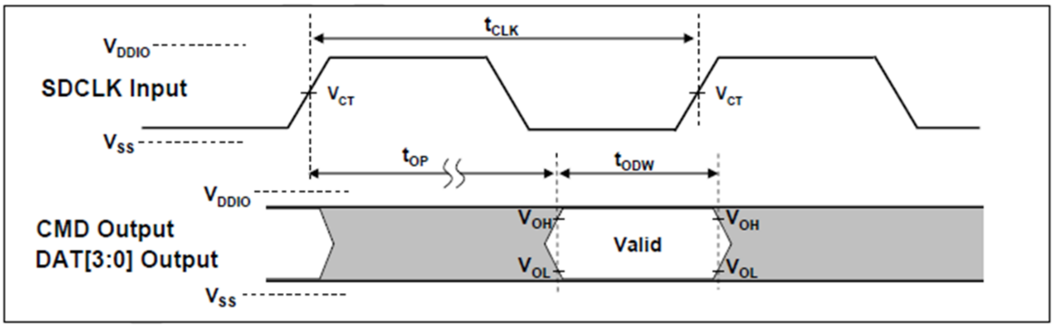

Figure 2-21. MSDC output timing diagram of variable window (SDR104)

Table 2-22. MSDC AC timing parameters of SDR12/SDR25/SDR50/SDR104 mode

Symbol	Min.	Max.	Unit	Remark
Clock CLK				
t_{CLK}	4.8	-	ns	208MHz (Max), Between rising edge, V_{CT}=0.975V
t_{CR}, t_{CF}	-	0.2*t_{CLK}	ns	t_{CR}, t_{CF} < 0.96ns (max) at 208MHz, C_{CARD}=10pF t_{CR}, t_{CF} < 2.00ns (max) at 100MHz, C_{CARD}=10pF The absolute maximum value of t_{CR}, t_{CF} is 10ns regardless of clock frequency.
Clock Duty	30	70	%	

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Symbol	Min.	Max.	Unit	Remark
Input CMD, DAT (SDR104)				
t_{IS}	1.40	-	ns	C_{CARD}=10pF, V_{CT}=0.975V
t_{IH}	0.80		ns	C_{CARD}=5pF, V_{CT}=0.975V
Input CMD, DAT (SDR50)				
t_{IS}	3.00	-	ns	C_{CARD}=10pF, V_{CT}=0.975V
t_{IH}	0.80	-	ns	C_{CARD}=5pF, V_{CT}=0.975V
Output CMD, DAT (SDR12/SDR25/SDR50)				
t_{ODLY}	-	7.5	ns	$t_{CLK} \geqq 10.0$ns, C_L=30pF, using driver type B, for SDR50
t_{ODLY}		14	Ns	$t_{CLK} \geqq 20.0$ns, C_L=40pF, using driver type B, for SDR25 and SDR12
T_{OH}	1.5	-	ns	Hold time at the t_{ODLY} (min), C_L=15pF
Output CMD, DAT (SDR104)				
t_{OP}	0	2	UI	Card output phase
Δt_{OP}	-350	+1550	ps	Delay varioation due to temperature change after tunung.
t_{ODW}	0.6	-	UI	t_{ODW}=2.88ns at 208MHz

2.2.5.6.4 DDR50 Speed Mode Timing

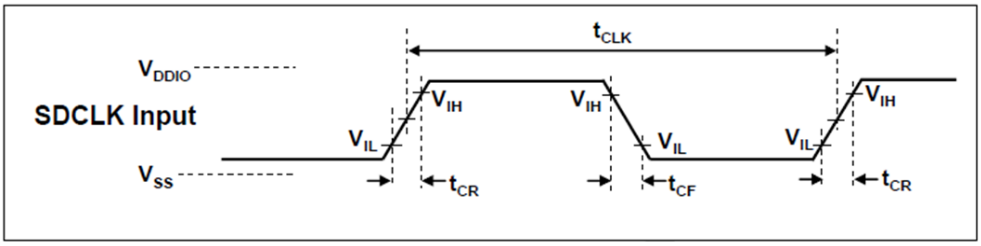

Figure 2-22. MSDC clock timing diagram of DDR50 speed mode

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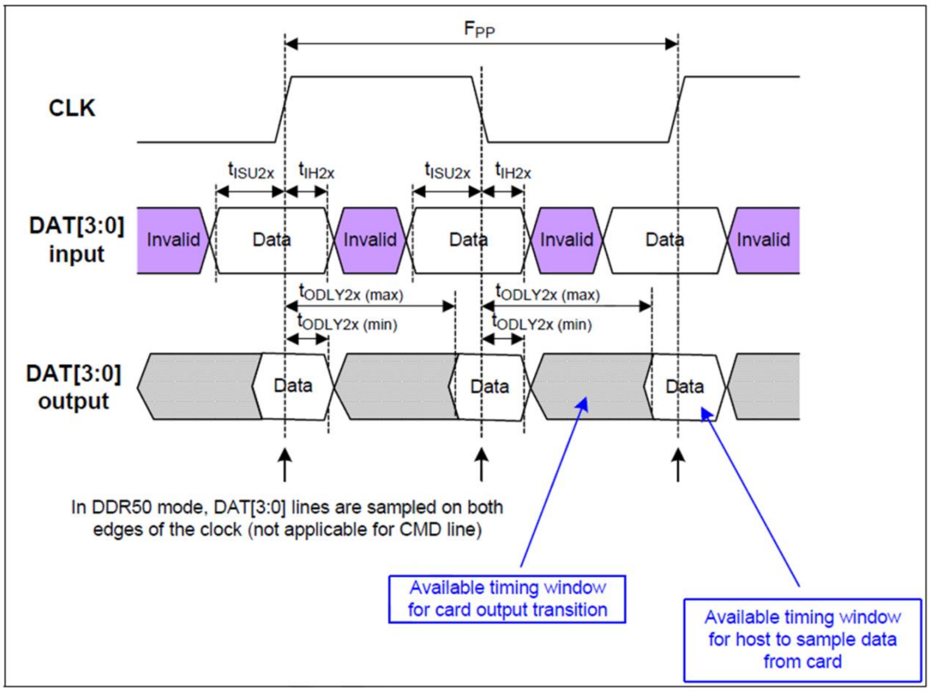

Figure 2-23. MSDC input/output timing diagram of DDR50 speed mode

Table 2-23. MSDC AC timing parameters of DDR50 speed mode

Parameter	Symbol	Min.	Max.	Unit	Remark
Input CMD (referenced to CLK rising edge)					
Input setup time	t_{ISU}	6	-	ns	C_{CARD}≦10pF (1 card)
Input hold time	t_{IH}	0.8	-	ns	C_{CARD}≦10pF (1 card)
Output CMD (referenced to CLK rising edge)					
Output delay time during data transfer mode	t_{ODLY}	-	13.7	ns	C_L≦30pF (1 card)
Output hold time	t_{OH}	1.5	-	ns	C_L≧15pF (1 card)
Input DAT (referenced to CLK rising and falling edge)					
Input setup time	t_{ISU}	3	-	ns	C_{CARD}≦10pF (1 card)
Input hold time	t_{IH}	0.8	-	ns	C_{CARD}≦10pF (1 card)
Output DAT (referenced to CLK rising and falling edge)					
Output delay time during data transfer mode	t_{ODLY}	-	7.0	ns	C_L≦25pF (1 card)
Output hold time	t_{OH}	1.5	-	Ns	C_L≧15pF (1 card)

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2.2.5.6.5 HS200 Speed Timing

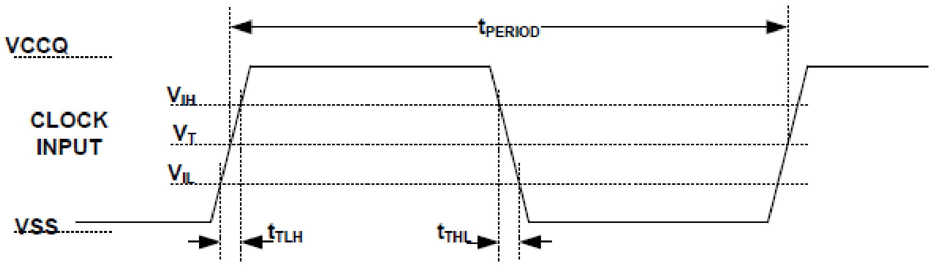
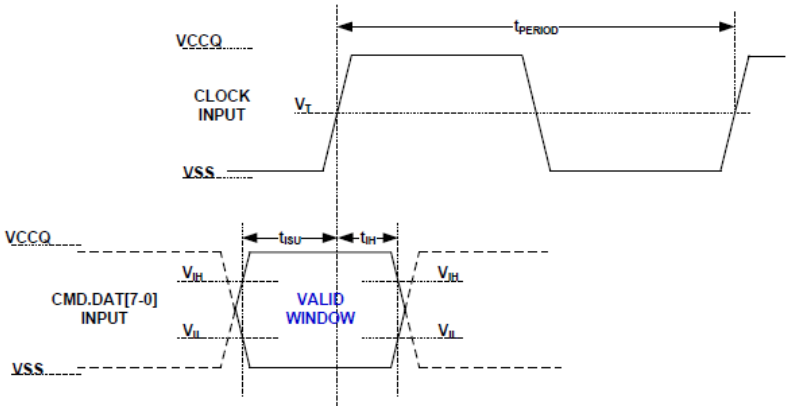


Figure 2-24. MSDC clock timing diagram of HS200



NOTE 1 t_{ISU} and t_{IH} are measured at V_{IL}(max.) and V_{IH}(min.).
NOTE 2 V_{IH} denote V_{IH}(min.) and V_{IL} denotes V_{IL}(max.).

Figure 2-25. MSDC input timing diagram of HS200

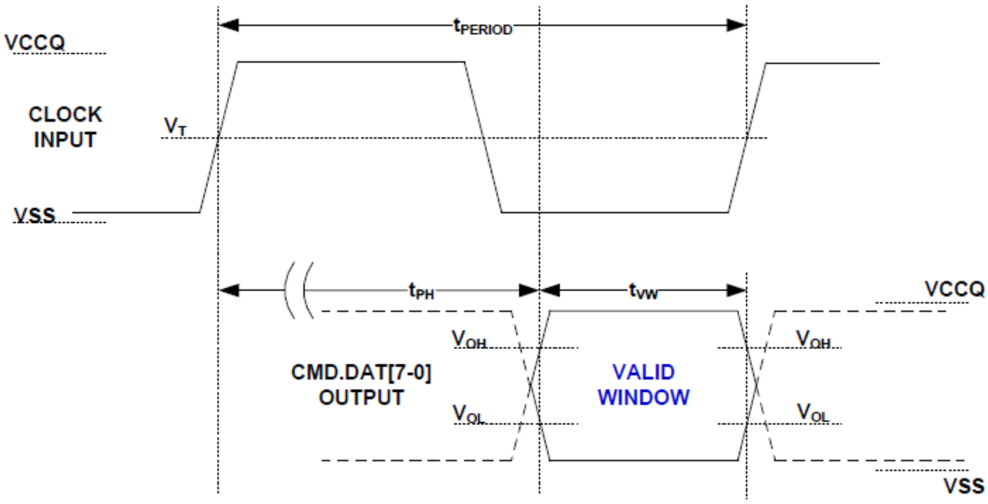


Figure 2-26. MSDC output timing diagram of HS200

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Table 2-24. MSDC AC timing parameters of HS200

Symbol	Min.	Max.	Unit	Remark
Clock CLK				
t_{PERIOD}	5	-	ns	200MHz (Max), between rising edge
t_{TLH}, t_{THL}	-	0.2 * t_{PERIOD}	ns	t_{TLH}, t_{THL} < 1ns (max) at 200MHz, C_{DEVICE}=6pF The absolute maximum value of t_{TLH}, t_{THL} is 10ns regardless of clock frequency.
Clock Duty	30	70	%	
Input CMD, DAT				
t_{ISU}	1.40	-	ns	$C_{DEVICE} \leqq 6$pF
t_{IH}	0.80		ns	$C_{DEVICE} \leqq 6$pF
Output CMD, DAT				
t_{PH}	0	2	UI	Device output momentary phase from CLK input to CMD or DAT lines output. Does not include a long term temperature drift.
ΔT_{PH}	-350 (ΔT=-20℃)	+1550 (ΔT=90℃)	ps	Delay variation due to temperature change after tunung. Total allowable shift of output valid window (T_{VW}) from last system Tuning procedure ΔT_{PH} is 2600ps for ΔT from -25°C to 125°C during operation.
t_{VW}	0.575	-	UI	t_{VW}=2.88ns at 208MHz
Note: Unit Interval (UI) is one bit nominal time. For example, UI=5ns at 200MHz.				

2.2.5.6.6 HS400 Speed Timing

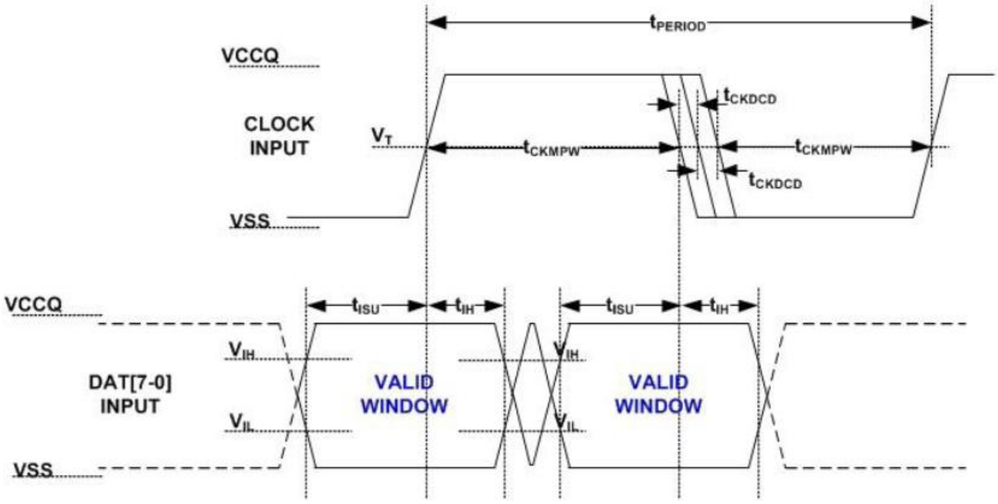

Figure 2-27. MSDC input timing diagram of HS400

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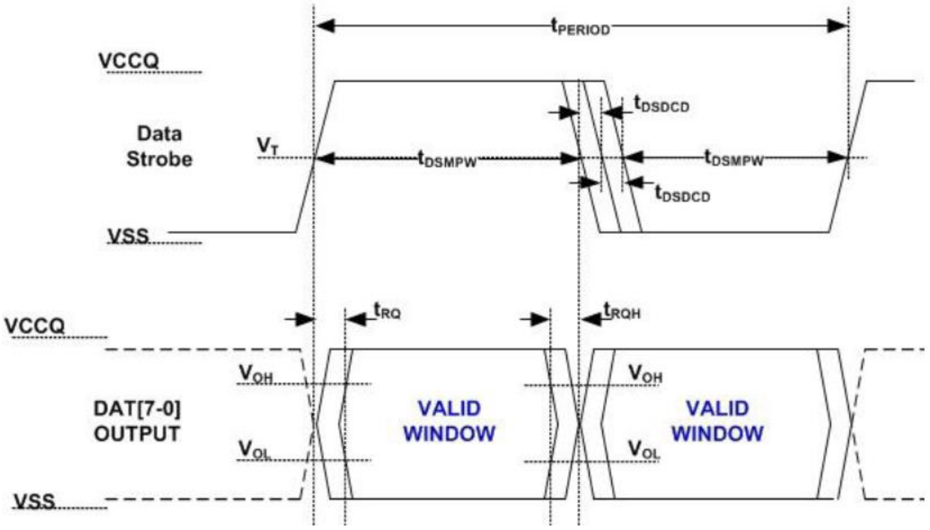

Figure 2-28. MSDC output timing diagram of HS400

Table 2-25. MSDC AC timing parameters of HS400

Parameter	Symbol	Min.	Max.	Unit	Remark
Input CLK					
Cycle time data transfer mode	t_{PERIOD}	5		ns	200MHz (max), between rising edges. With respect to V_T
Slew rate	SR	1.125		V/ns	With respect to V_{IH}/V_{IL}
Duty cycle distortion	t_{CKDCD}	0.0	0.3	ns	Allowable deviation from an ideal 50% duty cycle. With respect to V_T. Includes jitter, phase noise
Minimum pulse width	t_{CKMPW}	2.2		ns	With respect to V_T.
Input DAT (referenced to CLK)					
Input setup time	t_{ISUddr}	0.4		ns	$C_{Device} \leq$ 6pF. With respect to V_{IH}/V_{IL}
Input hold time	t_{IHddr}	0.4		ns	$C_{Device} \leq$ 6pF. With respect to V_{IH}/V_{IL}
Slew rate	SR	1.125		V/ns	With respect to V_{IH}/V_{IL}
Data Strobe					
Cycle time data transfer mode	t_{PERIOD}	5		ns	200MHz (max), between rising edges. With respect to V_T
Slew rate	SR	1.125		V/ns	With respect to V_{OH}/V_{OL} and HS400 reference load
Duty cycle distortion	t_{DSDCD}	0.0	0.2	ns	Allowable deviation from the input CLK duty cycle distortion (t_{CKDCD}). With respect to V_T. Includes jitter, phase noise
Minimum pulse width	t_{DSMPW}	2.0		ns	With respect to V_T.

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Parameter	Symbol	Min.	Max.	Unit	Remark
Read pre-amble	t_{RPRE}	0.4		t_{PERIOD}	Max value is specified by manufacturer. Value up to infinite is valid.
Read post-amble	t_{RPST}	0.4		t_{PERIOD}	Max value is specified by manufacturer. Value up to infinite is valid.
Input DAT (referenced to Data Strobe)					
Output skew	t_{RQ}		0.4	ns	With respect to V_{OH}/V_{OL} and HS400 reference load
Output hold skew	t_{RQH}		0.4	ns	With respect to V_{OH}/V_{OL} and HS400 reference load
Slew rate	SR	1.125		V/ns	With respect to V_{OH}/V_{OL} and HS400 reference load

2.2.5.7 SIM AC Timing Characteristics

Table 2-26. SIM AC timing parameters

Parameter	Conditions	Symbol	Min.	Typ.	Max.	Unit
SIM1_SCLK						
Rise and fall time	DVDD28_SIM1 = 1.8V	T_{rise_fall}	N/A	50	50	Ns
Clock duty		Duty	47	50	53	%
Rise and fall time	DVDD28_SIM1 = 3.0V	T_{rise_fall}	N/A	18	18	ns
Clock duty		Duty	47	50	53	%
SIM1_SIO						
Rise and fall time	DVDD28_SIM1 = 1.8V	T_{rise_fall}	N/A	50	1000	ns
Rise and fall time	DVDD28_SIM1 = 3.0V	T_{rise_fall}	N/A	50	1000	ns
SIM1_SRST						
Rise and fall time	DVDD28_SIM1 = 1.8V	T_{rise_fall}	N/A	18	1000	ns
Rise and fall time	DVDD28_SIM1 = 3.0V	T_{rise_fall}	N/A	18	1000	ns
SIM2_SCLK						
Rise and fall time	DVDD28_SIM2 = 1.8V	T_{rise_fall}	N/A	50	50	ns
Clock duty		Duty	47	50	53	%
Rise and fall time	DVDD28_SIM2 = 3.0V	T_{rise_fall}	N/A	18	18	ns
Clock duty		Duty	47	50	53	%
SIM2_SIO						
Rise and fall time	DVDD28_SIM2 = 1.8V	T_{rise_fall}	N/A	50	1000	ns
Rise and fall time	DVDD28_SIM2 = 3.0V	T_{rise_fall}	N/A	50	1000	ns
SIM2_SRST						
Rise and fall time	DVDD28_SIM2 = 1.8V	T_{rise_fall}	N/A	18	1000	ns
Rise and fall time	DVDD28_SIM2 = 3.0V	T_{rise_fall}	N/A	18	1000	ns

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2.3 System Configuration

2.3.1 Mode Selection

Table 2-27. Mode selection

Pin name	Description
KCOL0	0: Force USB download mode in bootrom 1: NA (default)
[0] AUD_DAT_MOSI [1] PWRAP_SPI0_CSN	00: Use CAM pins for legacy JTAG 01: Use MSDC1 pins for legacy JTAG 10: No dedicate JTAG 11: Use SPI pin for legacy JTAG

2.3.2 Constant Tie Pins

Table 2-28. Constant tied pins

Pin name	Description
TESTMODE	Test mode (tied to GND)

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2.4 Power-on Sequence

The power-on/off sequence is shown in the following figure:

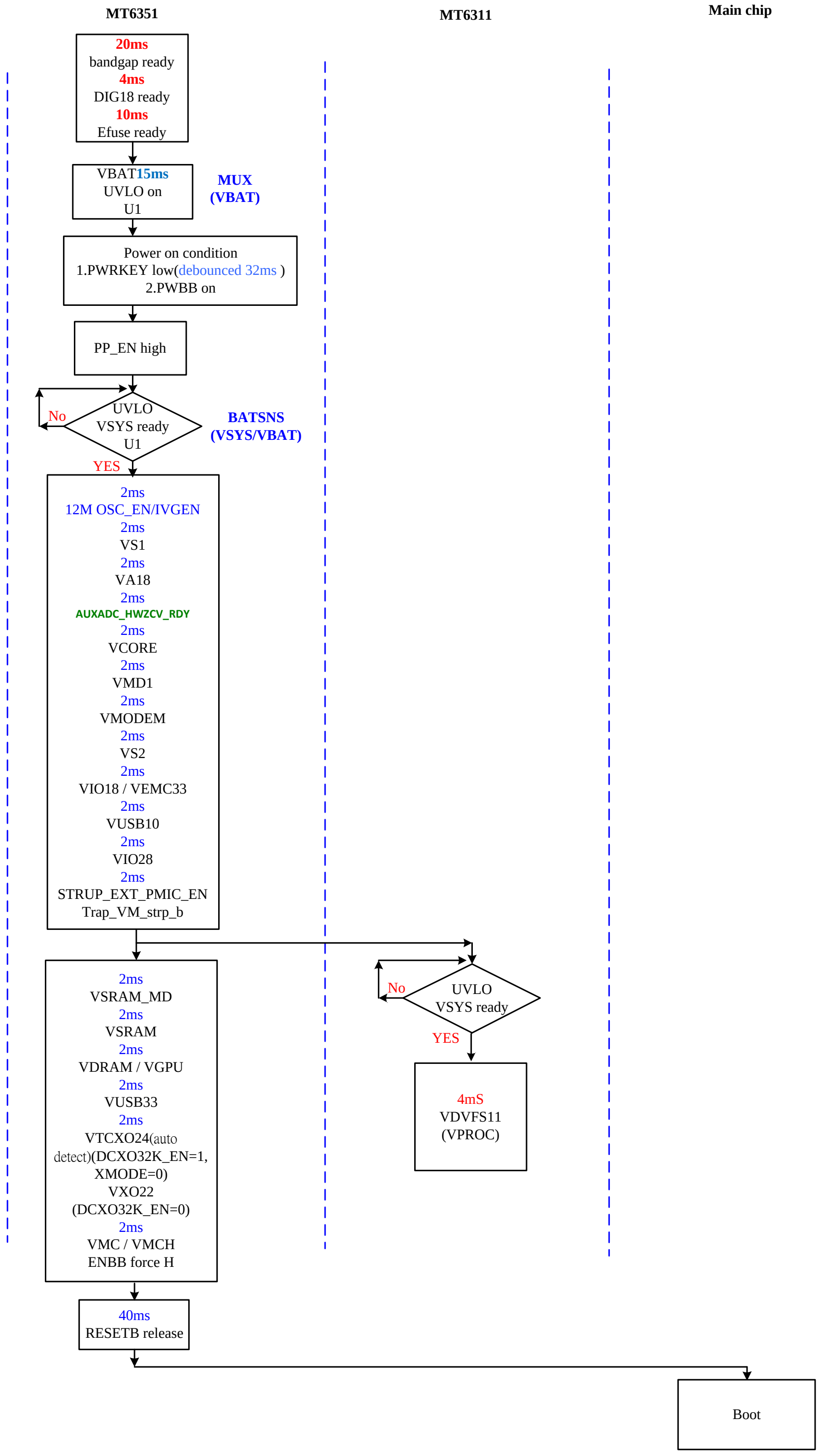

Figure 2-29. Power on sequence

Refer to PMIC datasheet for detailed timing sequence.

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2.5 Analog Baseband

2.5.1 Introduction

To communicate with analog blocks, a common control interface for all analog blocks is implemented. In addition, there are some dedicated interfaces for data transfer. The common control interface translates the APB bus write and read cycle for specific addresses related to analog front-end control. In the write or read of any of these control registers, there is a latency associated with the transfer of data to or from the analog front-end. Dedicated data interface of each analog block is implemented in the corresponding digital block. An analog block includes the following analog functions for the complete GSM/GPRS/WCDMA/LTE base-band signal processing:

- Base-band Rx: For I/Q channels base-band A/D conversion
- Base-band Tx: For I/Q channels base-band D/A conversion and smoothing filtering
- ETDAC: A DAC output to control buck-converter for envelop tracking technique.
- DETADC: A ADC that detects calibration, thermal data from RF chip.
- RF control: A DAC for automatic power control (APC) is included.The outputs are provided to external RF power amplifiers.
- Auxiliary ADC: Provides an ADC for auxiliary analog functions monitoring.
- Clock generation: One clock-squarer for shaping the input sinwave clock and 20 PLLs providing clock signals to base-band TRx, DSP, MCU, USB, MSDC units.

2.5.2 Features

The analog blocks include the following analog functions for complete GSM/GPRS/WCDMA base-band signal processing:

- BBRX
- BBTX
- ETDAC
- DETADC
- APC-DAC
- AUXADC
- Phase locked loop
- Temperature sensor

2.5.3 Block Diagram

2.5.3.1 BBRX

2.5.3.1.1 Block Descriptions

The receiver (Rx) performs baseband I/Q channels downlink analog-to-digital conversion:

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1. Analog input multiplexer: For each channel, a 2-input multiplexer is included.
2. A/D converter: 8 high performance sigma-delta ADCs perform I/Q digitization for further digital signal processing.

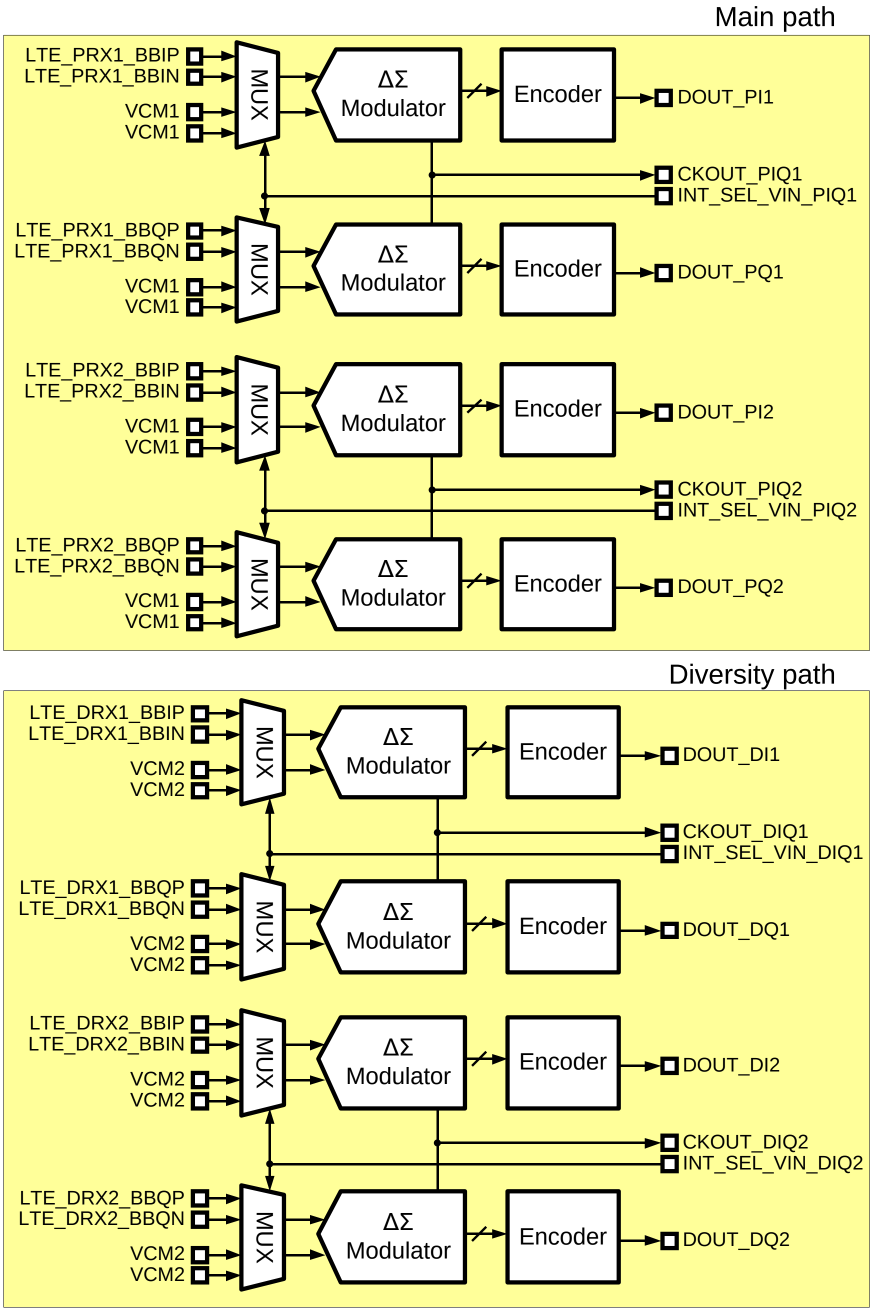

Figure 2-30. Block diagram of BBRX-ADC

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2.5.3.1.2 Functional Specifications

See the table below for the functional specifications of the base-band downlink receiver.

Table 2-29. Baseband downlink specifications

Symbol	Parameter	Min.	Typ.	Max.	Unit
VIN	Differential analog input voltage (peak-to-peak)			2.4	V
VCM	Common mode input voltage	0.65	0.7	0.75	V
FC	Input clock frequency	208		832	MHz
	Input clock duty cycle	49.5	50	50.5	%
RIN	Differential input resistance	2.8		20.8	kΩ
FS	Output sampling rate	208		832	MSPS
VOS	Differential input referred offset			10	mV
SIN	Signal to in-band noise	70		89	dB
AVDD	Analog power supply	1.7	1.8	1.9	V
T	Operating temperature	−20		80	°C
	Current consumption (per channel) – Power-up – Power-down		 12.3 10		 mA uA

2.5.3.2 BBTX

2.5.3.2.1 Block Descriptions

BBTX includes two channel DACs with the 1st order low pass filter. The DACs are PMOS current-steering topology with NMOS constant sinking current and the active RC filter performs current to voltage buffer.

The bitwidth of DACs is 11-bit which is encoded into 7 bits of thermometer code and 8 binary code by digital hard macro inside BBTX layout. The encoded bits are timing synchronized by D-type flip-flop which is toggled by the analog local clock. The MD-PLL delivers 832MHz differential clock to BBTX. A clock divider translates the 832MHz to 416MHz for DACs and AFIFO inside mixedsys.

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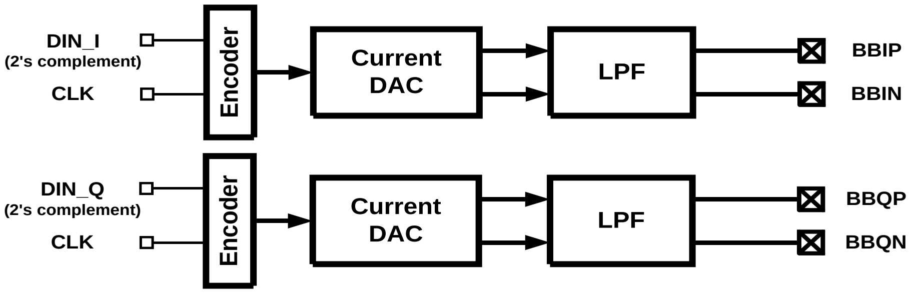

Figure 2-31. Block diagram of BBTX

2.5.3.2.2 Functional Specifications

Table 2-30. BBTX specifications

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{ocm}	DC output common mode voltage	0.615	0.65	0.685	V
V_{fs}	DAC output swing		2100		mV
N	DAC resolution		11.0		bit
F_s	Sampling clock		416		MHz
G_{mis}	3-sigma I/Q gain mismatch	-0.2		0.2	dB
V_{os}	3-sigma output differential DC offset			20	mV
F_{3dB}	3dB corner freq.		20/40		MHz
Dinb	Inband Droop		0.1		dB
DNL			1		LSB
INL			2		LSB
IM3	In-band two-tone test swing V1=V2=290/sqrt(2) mV		-58	-55	dBc
AVDD	Analog power supply	1.7	1.8	1.9	V
T	Operating temperature	-20		80	°C
	Current consumption (per channel) – Power-up – Power-down		 8 10		 mA uA

2.5.3.3 ETDAC

2.5.3.3.1 Block Descriptions

The ETDAC (Envelope Tracking DAC) provides analog envelope signal to external ET modulator. It includes:

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1. 11-bit D/A converter: Converts digital modulated signals to analog domain. The input to the DAC is sampled at 416MHz rate with the 11-bit resolution.
2. Smoothing filter: The low-pass filter performs smoothing function for DAC output signals with a 20/40MHz 1st-order Butterworth frequency response.

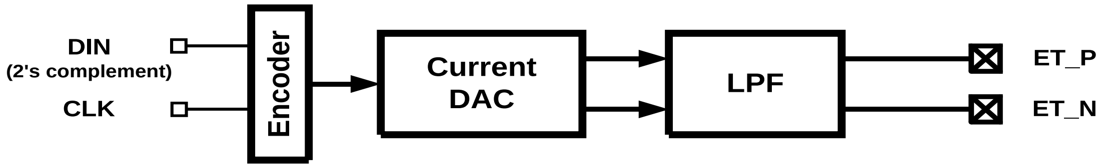

Figure 2-32. Block diagram of ETDAC

2.5.3.3.2 Functional Specfications

Table 2-31. ETDAC specifications

Symbol	Parameter	Min.	Typ.	Max.	Unit
N	Resolution		11		Bit
FS	Sampling rate		416		MSPS
IM3	3rd order Intermodulation distortion		-60	-50	dB
	Output swing (full swing)		2		Vppd
VOCM	Output CM voltage	0.6		0.85	V
	Output capacitance (single-ended)			10	PF
	Output resistance (differential)		100		KΩ
DNL	Differential nonlinearity	-1		+1	LSB
INL	Integral nonlinearity	-2		+2	LSB
FCUT	Filter -3dB cutoff frequency (calibrated)		20/40		MHz
AVDD	Analog power supply	1.7	1.8	1.9	V
T	Operating temperature	-20		80	°C
	Current consumption – Power-up – Power-down		 4.5 10		 mA uA

2.5.3.4 DETADC

2.5.3.4.1 Block Descriptions

The DETADC (DETection ADC) performs I/Q-channel path detections from RF chip:

1. Input buffer: For each channel, isolates RF signals from high-speed ADCs.

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2. 12-bit A/D converters: Convert the detected signals to 12-bit digital data sampled at 104MHz.

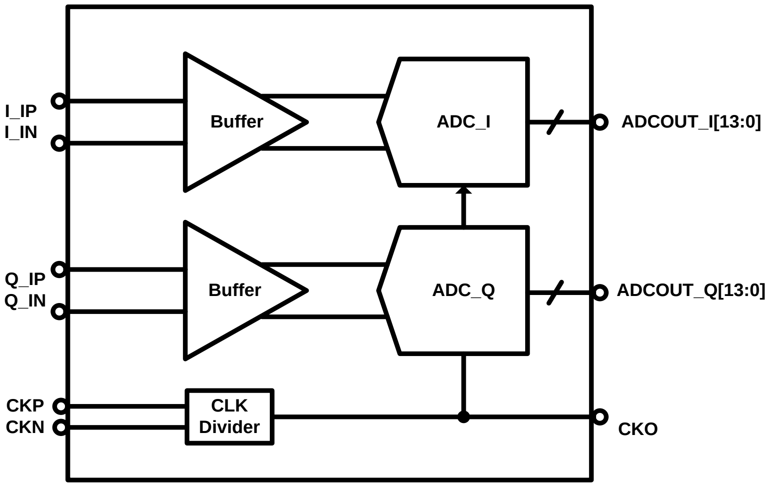

Figure 2-33. Block diagram of DETADC

2.5.3.4.2 Functional Specifications

See the table below for the functional specifications of DETADC

Table 2-32. DETADC specifications

Symbol	Parameter	Min.	Typ.	Max.	Unit
VIN	Analog input voltage (differential peak-to-peak)		1.2		V
VCM	Common mode input voltage		0.55		V
RIN	Input resistance	1.6	2	2.4	kΩ
CIN	Input capacitance		2	3	pF
FS	Sampling rate		104		MSPS
VOS	Differential input referred offset		30		mV
SNDR	Signal-to-noise-and-distortion ratio		60		dB
DR	Dynamic range		63		dB
THD	Total harmonic distortion		-66		dBc
AVDD	Analog power supply	1.7	1.8	1.9	V
T	Operating temperature	−20		80	°C
	Current consumption (per channel) – Power-up – Power-down		 6 1		 mA uA

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2.5.3.5 APC-DAC

2.5.3.5.1 Block Descriptions

See the figure below. APC-DAC is designed to produce a single-ended output signal at APC pin.

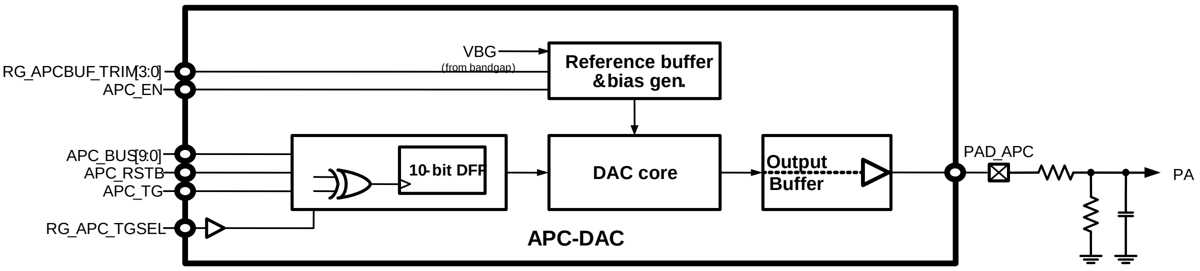

Figure 2-34. Block diagram of APC-DAC

2.5.3.5.2 Functional Specifications

See the table below for the functional specifications of the APC-DAC.

Table 2-33. APC-DAC specifications

Symbol	Parameter	Min.	Typ.	Max.	Unit
N	Resolution		10		Bit
F_S	Clock rate	1.0833		2.1666	MS/s
T_S	Settling time (99% full-swing settling)			5	us
$V_{O,max}$	Maximum output			AVDD – 0.2	V
C_L	Output loading capacitance		220	2200	pF
DNL	Differential nonlinearity (code 30 ~ 970)		±1.0		LSB
INL	Integral nonlinearity (code 30 ~ 970)		±2.0		LSB
AVDD	Analog power supply	2.6	2.8	3.0	V
T	Operating temperature	−20		85	°C
	Current consumption – Power-up – Power-down		 450 20		 uA uA

2.5.3.6 AUXADC

2.5.3.6.1 Block Descriptions

The auxiliary ADC includes the following functional blocks:

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1. Analog multiplexer: Selects signal from one of the auxiliary input channels. There are 16 input channels of AUXADC. Some are for internal voltage measurement and some for external voltage measurement. Environmental messages to be monitored, e.g. temperature, should be transferred to the voltage domain.
2. 12-bit A/D converter: Converts the multiplexed input signal to 12-bit digital data.

Table 2-34. AUXADC channels

AUXADC channel ID	Description
Channel 0	External use (AUX_IN0)
Channel 1	External use (AUX_IN1)
Channel 2	External use (AUX_IN2)
Channel 3	External use (AUX_IN3)
Channel 4	External use (AUX_IN4)
Channel 5	NA
Channel 6	NA
Channel 7	NA
Channel 8	NA
Channel 9	NA
Channel 10	Internal use
Channel 11	Internal use
Channel 12	NA
Channel 13	NA
Channel 14	NA
Channel 15	NA

2.5.3.6.2 Functional Specifications

See the table below for the functional specifications of auxiliary ADC.

Table 2-35. AUXADC specifications

Symbol	Parameter	Min.	Typ.	Max.	Unit
N	Resolution		12		Bit
FC	Clock rate		3.25		MHz
FS	Sampling rate @ N-Bit		3.25/(N+8)		MSPS
	Input swing	0.05		1.45	V
CIN	Input capacitance Unselected channel Selected channel (PAD loading excluded)		 50 4		 fF pF
	Clock latency		N+8		1/FC
DNL	Differential nonlinearity		+1.0/-1.0		LSB
INL	Integral nonlinearity		+2.0/-2.0		LSB

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Symbol	Parameter	Min.	Typ.	Max.	Unit
AVDD	Analog power supply	1.7	1.8	1.9	V
T	Operating temperature	-20		80	°C
	Accuracy			+-10	mV

2.5.3.7 Clock Squarer

2.5.3.7.1 Block Descriptions

For most VCXO, the output clock waveform is sinusoidal with too small amplitude (about several hundred mV) to make digital circuits function well. The clock squarer is designed to convert such a small signal to a rail-to-rail clock signal with excellent duty-cycle.

2.5.3.7.2 Functional Specifications

See the table below for the functional specifications of clock squarer.

Table 2-36. Clock squarer specifications

Symbol	Parameter	Min.	Typ.	Max.	Unit
Fin	Input clock frequency	13	26		MHz
Fout	Output clock frequency	13	26		MHz
Vin	Input signal amplitude	350	500	1,000	mVpp
DcycIN	Input signal duty cycle		50		%
DcycOUT	Output signal duty cycle	DcycIN-5		DcycIN+5	%
TR	Rise time on pin CLKSQOUT			5	ns/pF
TF	Fall time on pin CLKSQOUT			5	ns/pF
	Maximum Positive Overshoot			1.98	V
	Minimum Negative Overshoot	-0.1			V
AVDD	Analog power supply	1.7	1.8	1.9	V
T	Operating temperature	-20		80	°C
	Current consumption		650		uA

2.5.3.8 Temperature Sensor

2.5.3.8.1 Block Descriptions

In order to monitor the temperature of CPUs, several temperature sensors are provided. The temperature sensor is made of substrate BJT in the CMOS process. The voltage output of temperature sensor is measured by AUXADC.

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2.5.3.8.2 Functional Specifications

See the table below for the functional specifications of temperature sensor.

Table 2-37. Temperature sensor specifications

Symbol	Parameter	Min.	Typ.	Max.	Unit
	Resolution		0.15		°C
	Temperature range	0		85	°C
	Accuracy	-5		5	°C
	Active current		60		uA
	Quiescent current		10		uA

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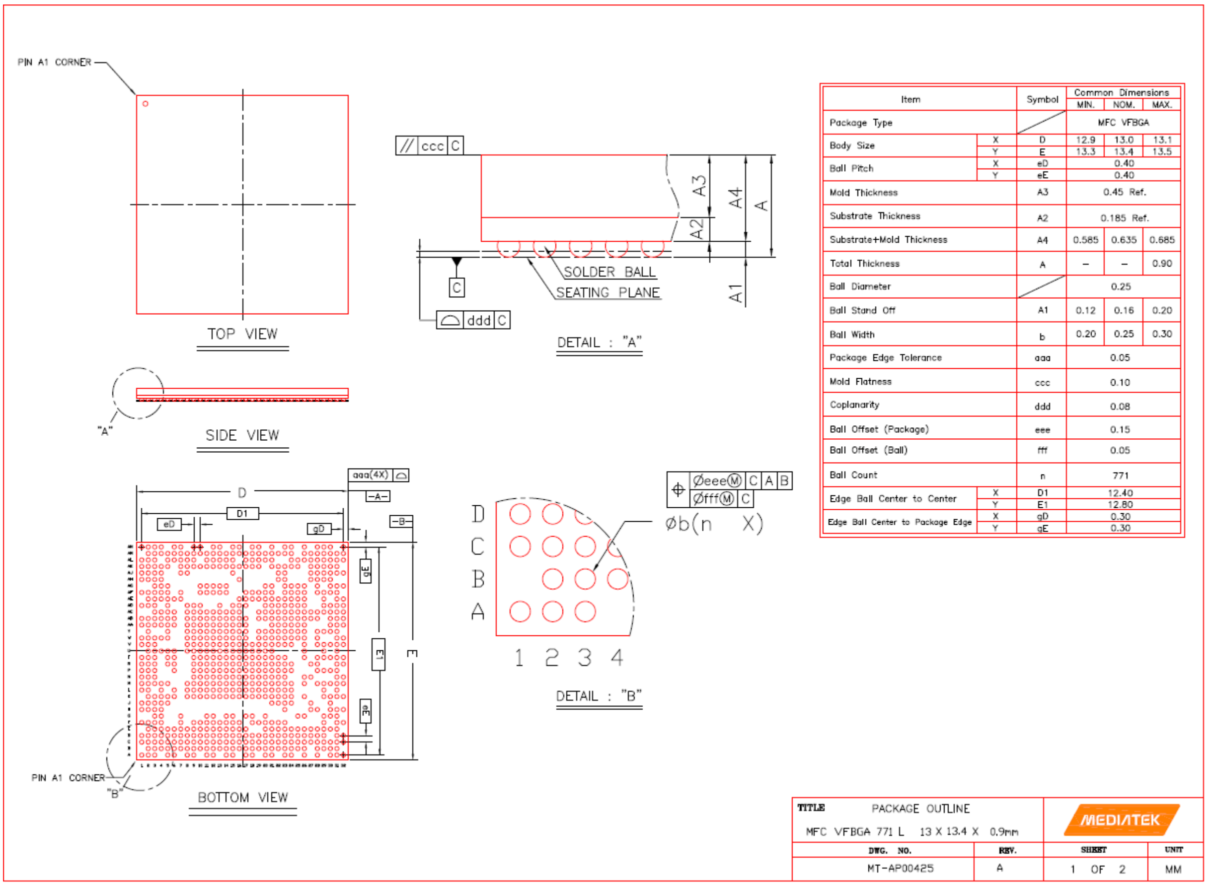
2.6 Package Information

2.6.1 Package Outlines



Item		Symbol	Common Dimensions MIN.	NOM.	MAX.
Package Type			MFC VFBGA		
Body Size	X	D	12.9	13.0	13.1
	Y	E	13.3	13.4	13.5
Ball Pitch	X	eD	0.40		
	Y	eE	0.40		
Mold Thickness		A3	0.45 Ref.		
Substrate Thickness		A2	0.185 Ref.		
Substrate+Mold Thickness		A4	0.585	0.635	0.685
Total Thickness		A	–	–	0.90
Ball Diameter			0.25		
Ball Stand Off		A1	0.12	0.16	0.20
Ball Width		b	0.20	0.25	0.30
Package Edge Tolerance		aaa	0.05		
Mold Flatness		ccc	0.10		
Coplanarity		ddd	0.08		
Ball Offset (Package)		eee	0.15		
Ball Offset (Ball)		fff	0.05		
Ball Count		n	771		
Edge Ball Center to Center	X	D1	12.40		
	Y	E1	12.80		
Edge Ball Center to Package Edge	X	gD	0.30		
	Y	gE	0.30		

*Figure 2-35. Outlines and dimensions of VFBGA 13mm*13.4mm, 771-ball, 0.4mm pitch package*

2.6.2 Thermal Operating Specifications

Table 2-38. Thermal operating specifications

Symbol	Description	Value	Unit	Note
	Max. operating junction temperature	125	°C	
	Package thermal resistances in nature convection	37.65	°C/Watt	

2.6.3 Lead-free Packaging

The chip is provided in a lead-free package and meets RoHS requirements.

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2.6.4 MSL

MSL of this chip is 3.

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2.7 Power Delivery Network

Table 2-39. PDN specifications

Power rail	R_{DC} (mohm)	Remote_R_{DC} (mohm)	Low frequency band ZAC (mΩ) @ low frequency band	High frequency band ZAC (mΩ) @ high frequency band
VCORE	23	1.8	25.0@0.2 -> 25.0@10MHz	25.0@10 -> 58.0@30MHz
DVFS1	9.6	0.8	9.7@0.2 -> 9.7@10MHz	9.7@10 -> 81.0@100MHz
VSRAM	130		130.0@0.0 -> 130.0@5MHz	130.0@5 -> 4700.0@50MHz
VEMI (DDR)	40		40.0@0.0 -> 40.0@45MHz	40.0@45 -> 210.0@250MHz
VGPU	20	1.6	25.0@0.2 -> 25.0@9MHz	25.0@9 -> 140.0@55MHz
VMD1	60	4.8	50.0@0.2 -> 50.0@10MHz	50.0@10 -> 130.0@20MHz
VMDSRAM	60	4.8	59.0@0.2 -> 59.0@12MHz	59.0@12 -> 350.0@90MHz
VMODEM	51	4	50.0@0.2 -> 50.0@10MHz	50.0@10 -> 500.0@20MHz

Note: Refer to document "MT6757_PDN_Checking_Notice.pdf" on DCC for more design concepts.

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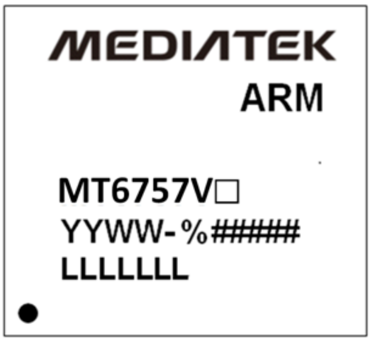
2.8 Ordering Information

2.8.1 Top Marking Definition



- □: “-E” Engineering sample
- YYWW: Date code
- #####: Subcontractor code
- LLLLLLL: Die lot No.

Figure 2-36. Top marking of MT6757

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